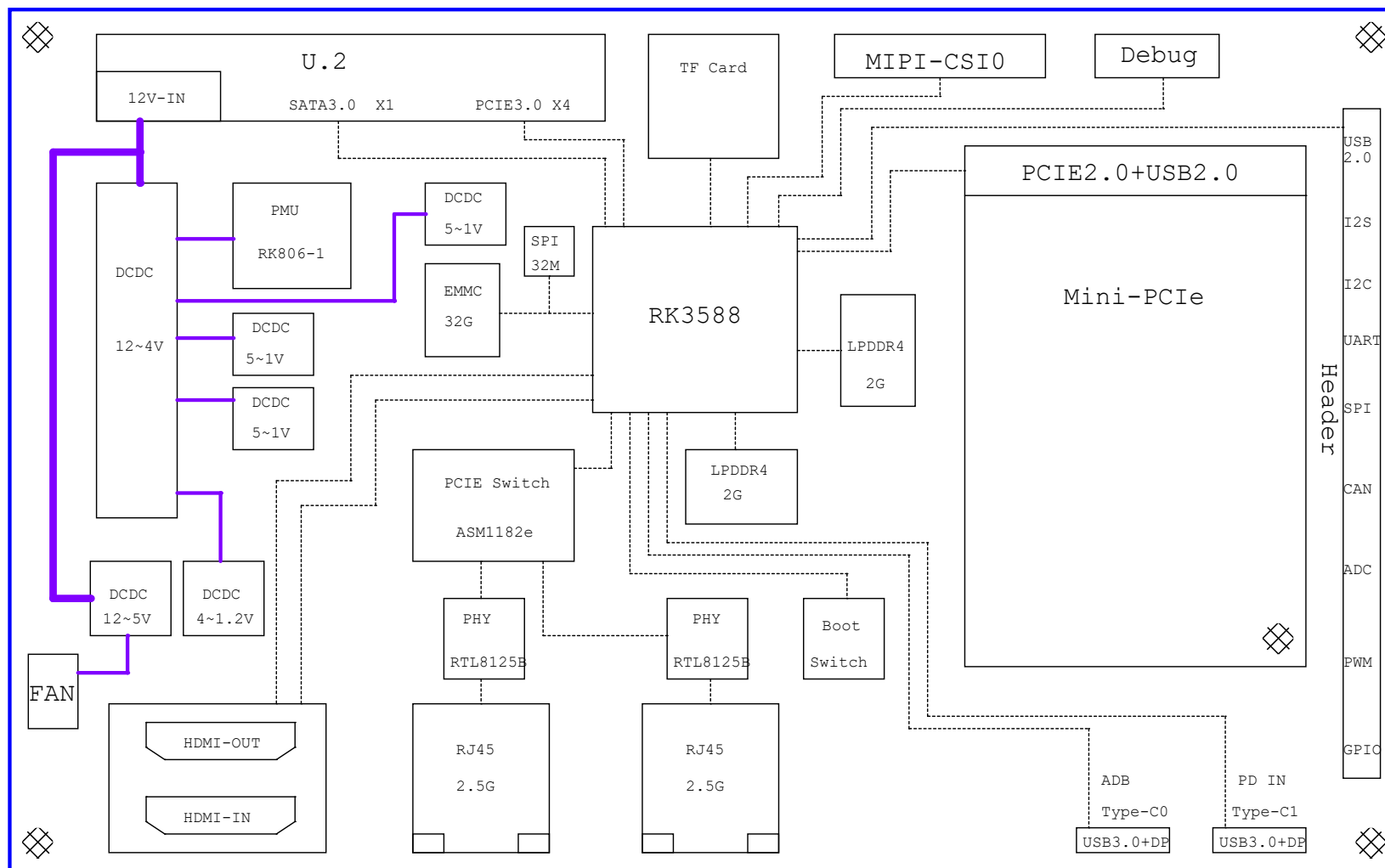
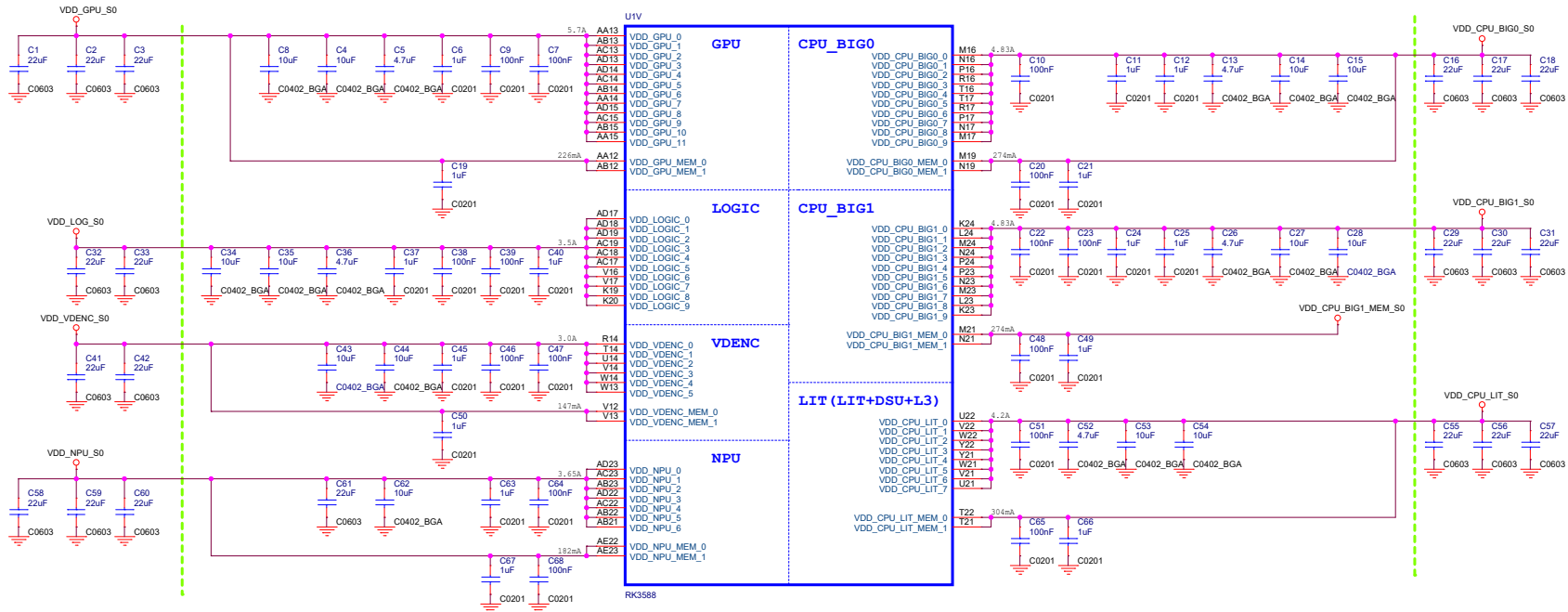


Revision History

Version	Date	By	Change Dscription	Approved
V1.0.0	2022-3-18	Phi	1:Revision preliminary version	
V1.1.0	2022-8-12	Phi	1.串口RX增加二极管，防外部漏电到芯片。 2.PCIE时钟芯片更换成Au5426，输出4路时钟，其中主芯片供两路，外部供两路。备用跳线主从两种选择。 3.匹配U.2底板，增加POWER_ON,RESET,调试串口，DET检测脚。 4.两路输入电源，以大电压关闭小电压，关闭后只有一路电源可用，与edge2相同。 5.去掉所有5V不启动选择，5V正常启动。：4V，5V，PCIE座子3个电源。 6.ASM8211E配置修改GPIO1去掉下拉 7.增加U.2输出5V 8.修正SATA线序 9.LED灯改成关机不亮,灯改成蓝色，封装位置不变 10.风扇改成4PIN调速5V,风扇电源使能默认上拉打开	



RK3588_V (POWER)



RK3588_E (OSC/PLL/PMUIO1/2)

Note:

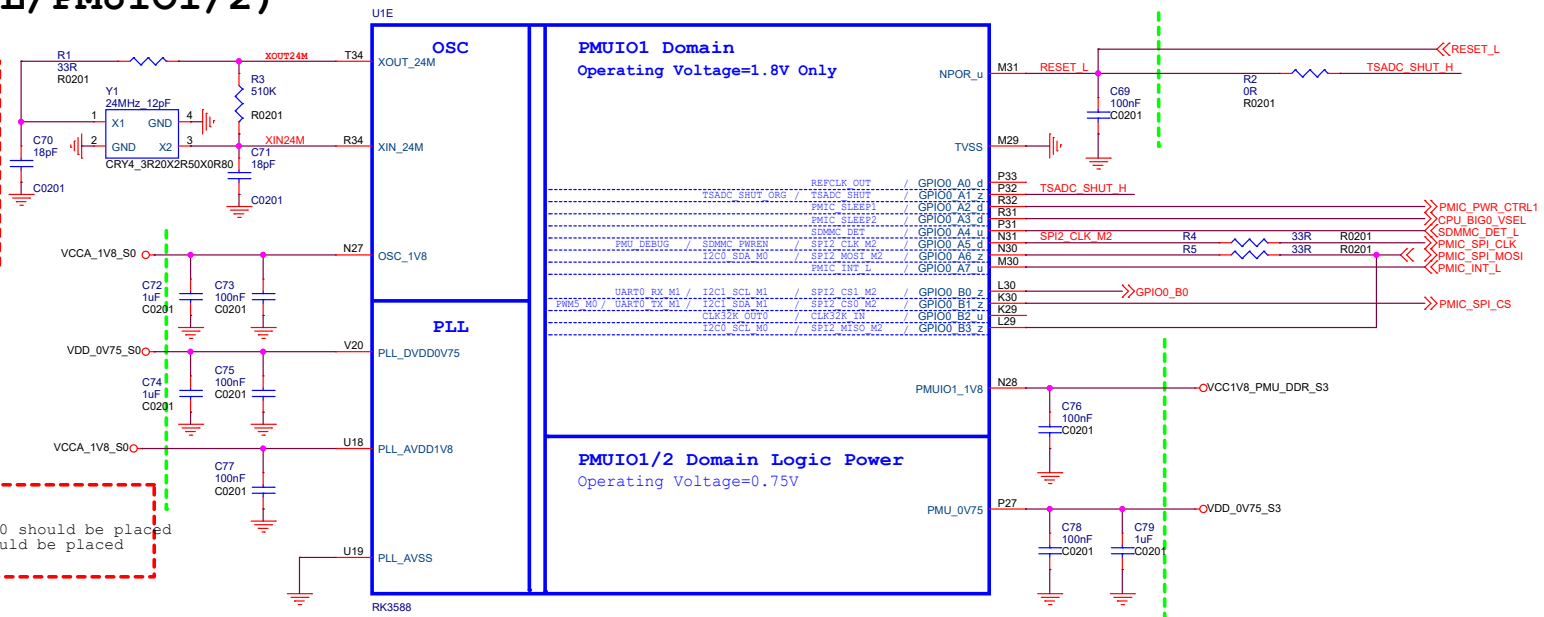
Adjusted the load capacitance according to the crystal specification

The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

$CL = (CL1 * CL2 / (CL1 + CL2)) + PCB \text{ strays}$
Total CL=12pF

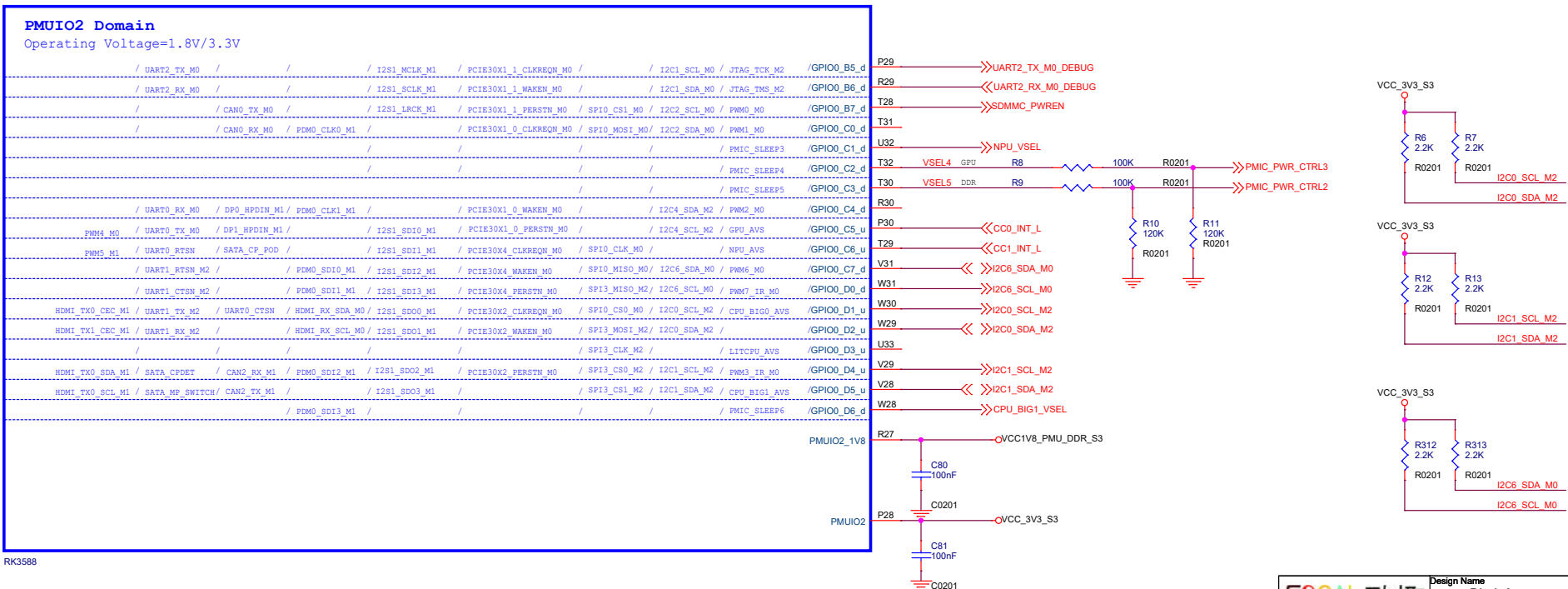
Note:

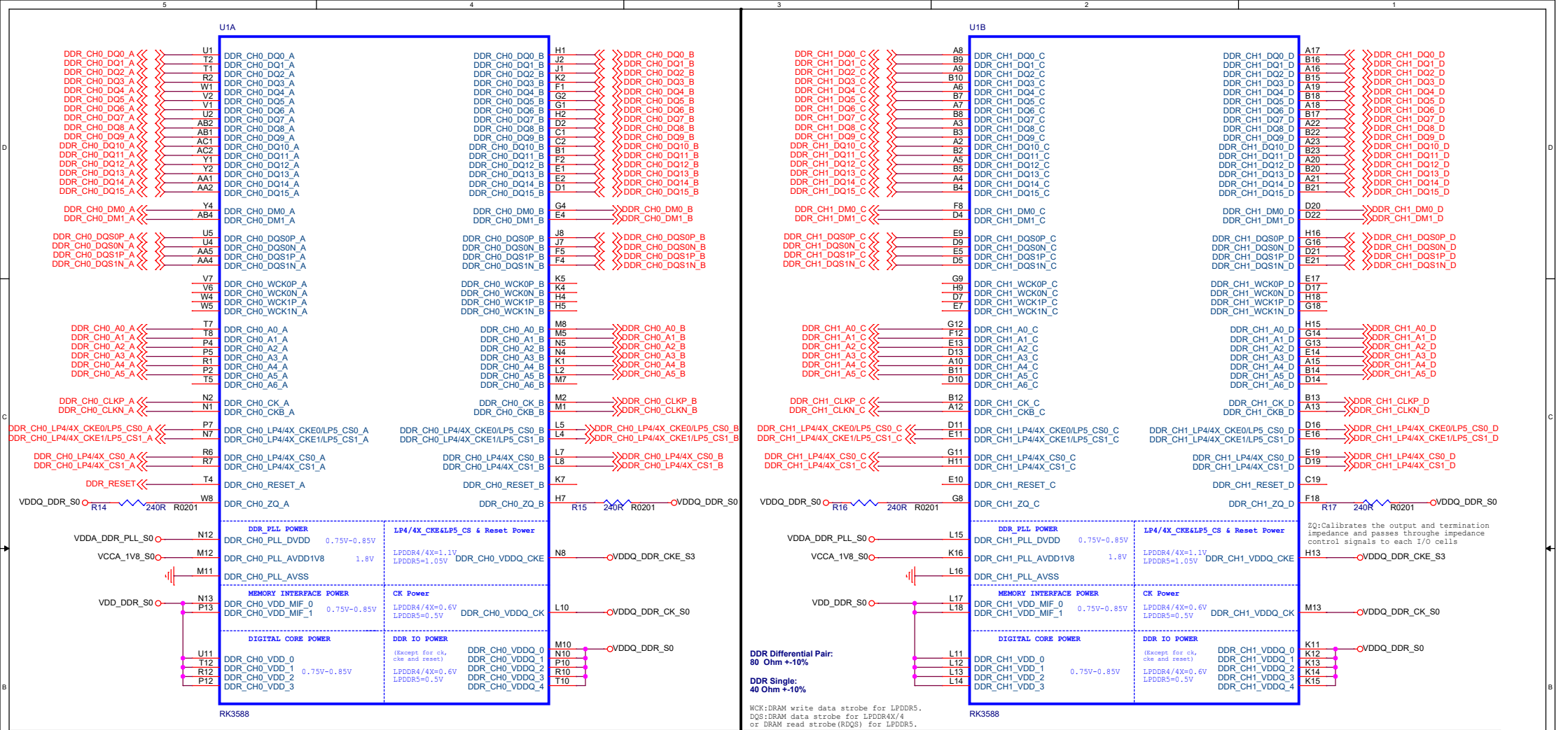
The Caps between green line and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package



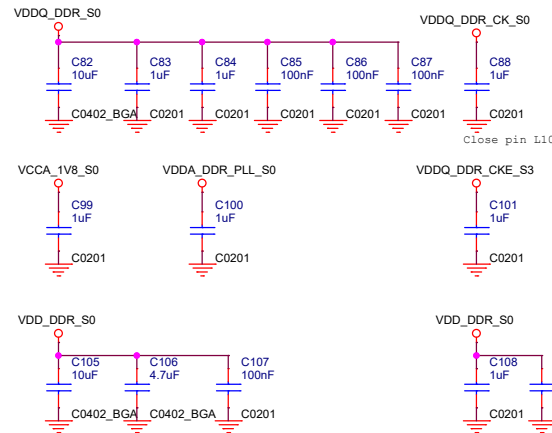
RK3588_F (PMUIO2)

U1F



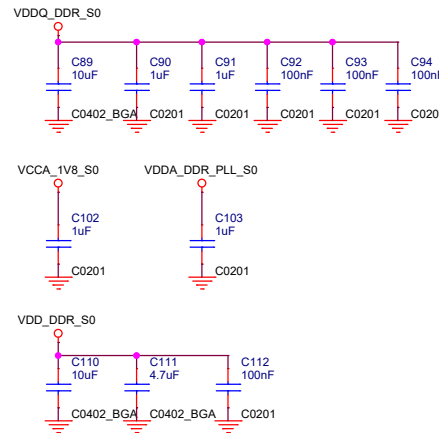


DDR FILTER



Hold power of CLK during retention times.

Sequence:
VDD-VDDQ_CKE-VDDQ
VDDQ_LP4/4X_CKE/LP5_CS:
power for LP4_CKE/LP5_CS and RESET.
lpddr4x=1.1V/lpddr5=1.05V
VDDQ_CK power for CK,
LPDDR4/4X=0.6V/LPDDR5=0.5V
VDDQ_Power for DDR IO(except for ck,
cke and reset);
LPDDR4/4X=0.6V/LPDDR5=0.5V



Design Name		Blade3	
Size	Page Name	Rev	
Custom	06.RK3588 DDR Controller	V1.1.0	
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U1C



U1D



Size	Page Name	Rev
Custom	08.RK3588 USB30/USB20 Ctrl	V1.1.0
Date:	Wednesday, September 28, 2022	Sheet 8 of 26

VCCI01 Domain
Operating Voltage=1.8V

SPI4 MISO M0 / UART3 RX M0 /	I2C3 SDA M0 /				G29
SPI4 MOSI M0 / UART3 TX M0 /	I2C3 SCL M0 /				G27
SPI4 CLK M0 / UART3 BSW /	I2C6 SDA M1 /	I2S0 MCLK			F30
SPI4 CS0 M0 / UART3 CS0 /	I2C6 SCL M1 /	I2S0 SCLK			E30
SPI4 CS1 M2 / UART4 BSW /	I2C5 SDA M2 /	I2S0 MCLK M0 /			E31
SPI4 CS2 M2 / UART4 CS2 /	I2C5 SCL M2 /	I2S0 SCLK			E30
SPI4 CS3 M2 / UART4 CS3 /	I2C5 SDA M3 /	I2S0 MCLK M0 /			E31
SPI4 CS4 M2 / UART4 CS4 /	I2C5 SCL M3 /	I2S0 SCLK			E29
SPI4 CS5 M2 / UART4 CS5 /	I2C4 SDA M4 /	FGM0 CLK0 M0 /			E29
SPI4 CS6 M2 / UART4 CS6 /	I2C4 SCL M4 /	I2S0 SCLK			E29
SPI1 MISO M2 / UART6 TX M2 /	I2C7 SCL M0 /	I2S0 SD01			F28
SPI1 MOSI M2 / UART6 RX M2 /	I2C7 SDA M0 /	FGM0 SD11 M0 /	I2S0 SD02 / I2S0 SD03		F27
SPI1 CLK M2 / UART6 TX M0 /	I2C1 SCL M4 /	FGM0 SD12 M0 /	I2S0 SD03 / I2S0 SD12		F28
SPI1 CS0 M2 / UART6 CS0 M0 /	I2C1 SDA M4 /	FGM0 SD13 M0 /	I2S0 SD13		E28
SPI1 CS1 M2 / UART6 CS1 M0 /	I2C1 SCL M4 /	FGM0 SD14 M0 /	I2S0 SD14		E28
SPI1 CS2 M2 / UART6 CS2 M0 /	I2C1 SDA M4 /	FGM0 SD15 M0 /	I2S0 SD15		D28
SPI1 CS3 M2 / UART6 CS3 M0 /	I2C1 SCL M4 /	FGM0 SD16 M0 /	I2S0 SD16		G26

⚡ HDMI_0X_01_DET_L

VCCI01_1V8

G20

C137
100nF

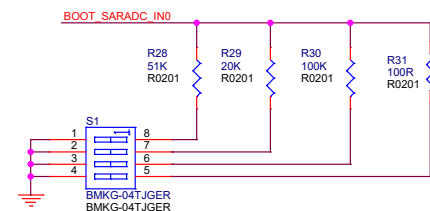
GND

C0201

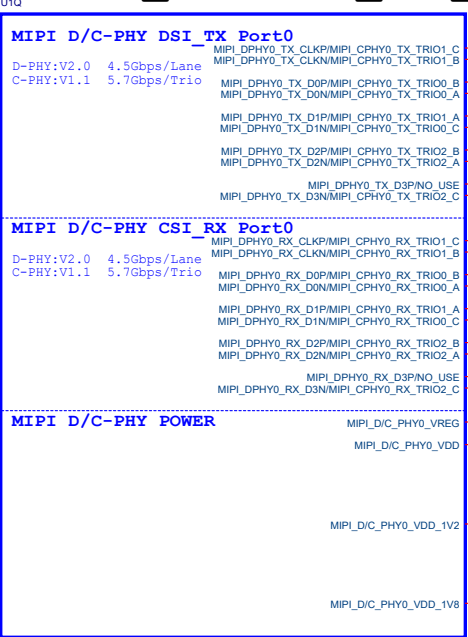
VCC_1V8_S0

[illegible][illegible]

	Item	Rup	Rdown	ADC	VOL	BOOT MODE
	LEVEL1	DNP	100K	0	0V	USB (Maskrom mode)
	LEVEL2	100K	20K	682	0.3V	SD Card-USB
	LEVEL3	100K	51K	1365	0.6V	EMMC-USB (Default)
	LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
	LEVEL5	100K	200K	2730	1.2V	FSPI M1-USB
	LEVEL6	100K	499K	3412	1.5V	FSPI M2-USB
	LEVEL7	100K	DNP	4095	1.8V	FSPI M2-FSPI M1-FSPI M0-EMMC-SD Card-USB

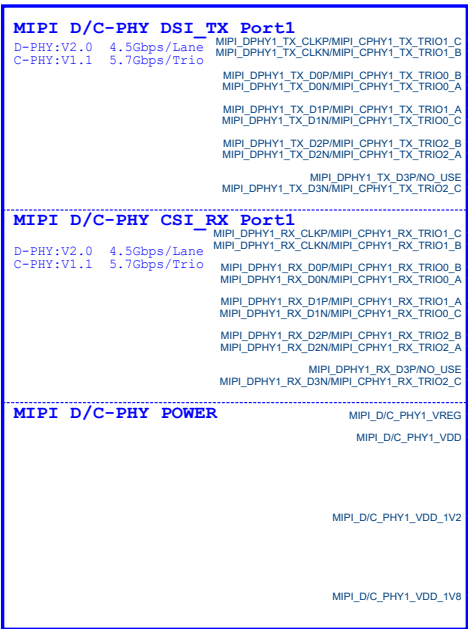


RK3588_Q/R (MIPI_D/C_PHY0/1)



RK3588

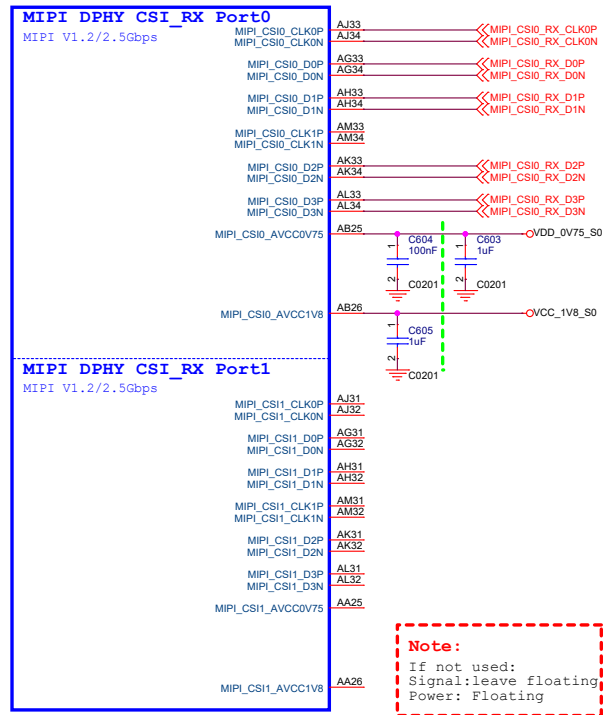
U1R



RK3588

Note:
If not used:
Signal:leave floating
Power: Floating

RK3588_P (MIPI_DPHY_CSI_RX_PHY)



RK3588

MIPI_CSI_RX Configuration

Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane +	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
	Sensor2 x2Lane	MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3, but clock lane1 is invalid; In dual clock lanes mode, CLK0P/0N is the clock lane of Data lane0 and Data lane1, while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
The Caps to the left of green line should be placed under the U1000 package. Other caps should be placed close to the U1000 package.



Design Name		Blade3	
Size	Custom	Page Name	10_RK3588_MIPI_Interface
Date	Wednesday, September 28, 2022	Rev	V1.1.0
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RK3588_S (HDMI2.1 TX)

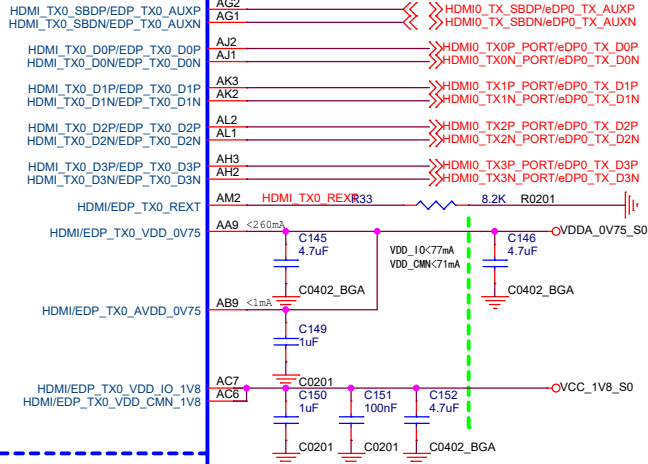
Note:

The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

U1S

HDMI TX/eDP MUX Port0

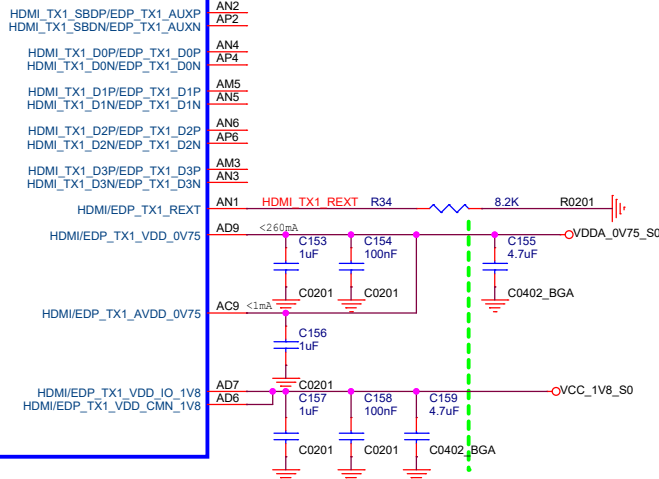
HDMI:V2.1 12Gbps
eDP: V1.3 5.4Gbps



HDMI2.1_TX
100 Ohm +-10%

HDMI TX/eDP MUX Port1

HDMI:V2.1 12Gbps
eDP: V1.3 5.4Gbps



Note:

The Caps to the left of green line should be placed under the U1000 package. Other caps should be placed close to the U1000 package.

Note:

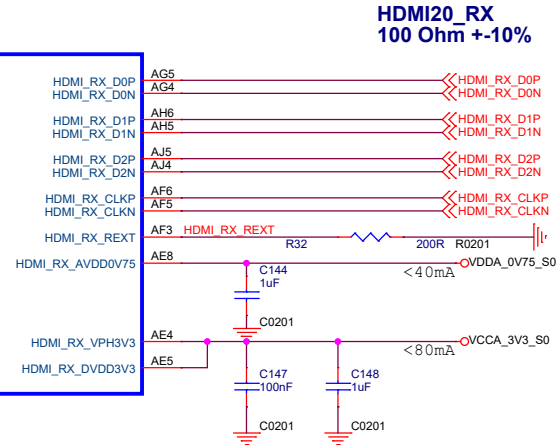
If not used:
Signal: leave floating
Power: Floating or tie to VSS

RK3588_T (HDMI20 RX)

U1T

HDMI RX

HDMI: V2.0



HDMI20_RX
100 Ohm +-10%

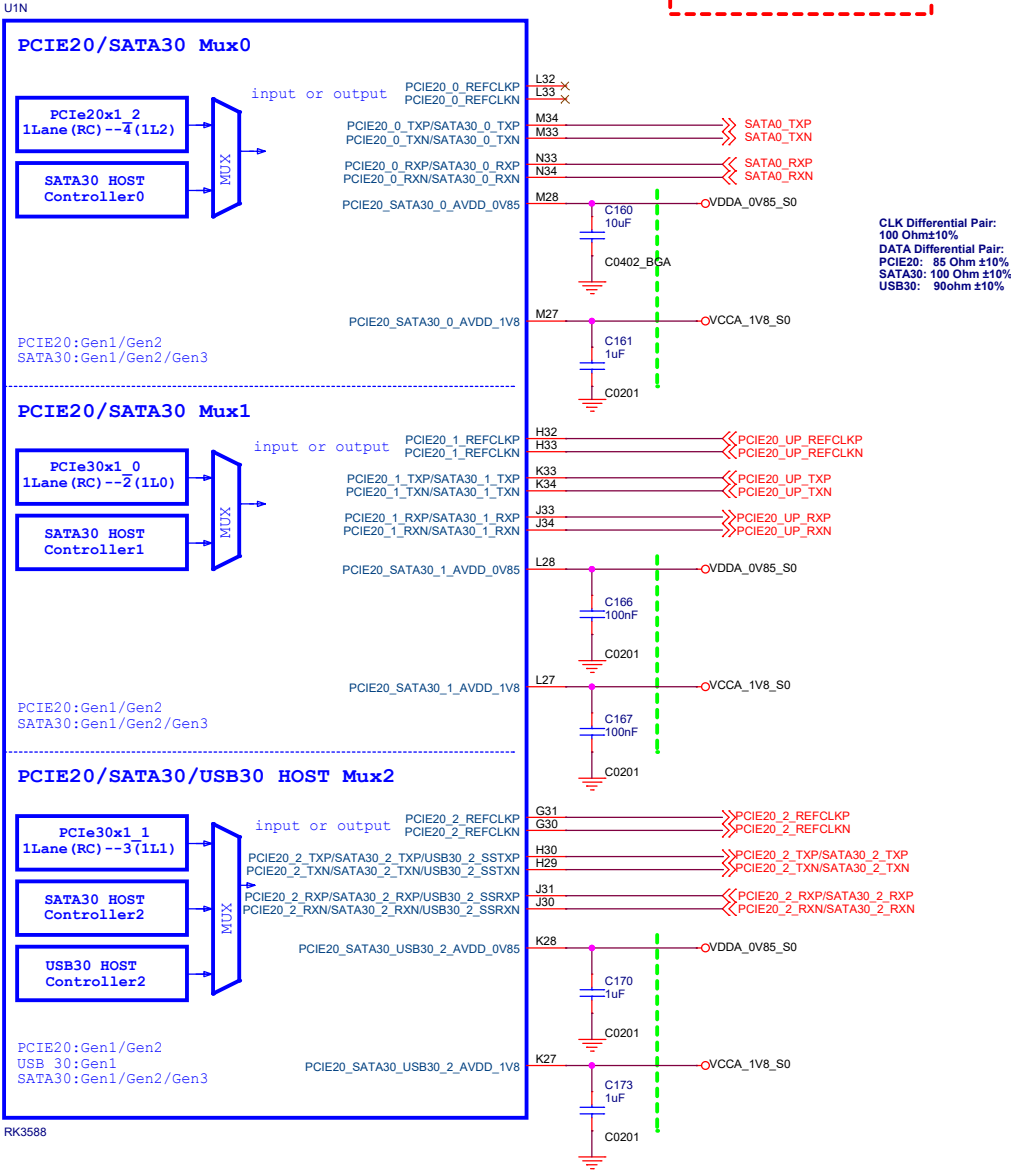
Note:

If not used:
Signal: leave floating
Power: Floating



Design Name		Blade3	
Size	Page Name	Rev	
Custom	11.RK3588 HDMI/eDP Interface	V1.1.0	
Date:	Wednesday, September 28, 2022	Sheet	11 of 26

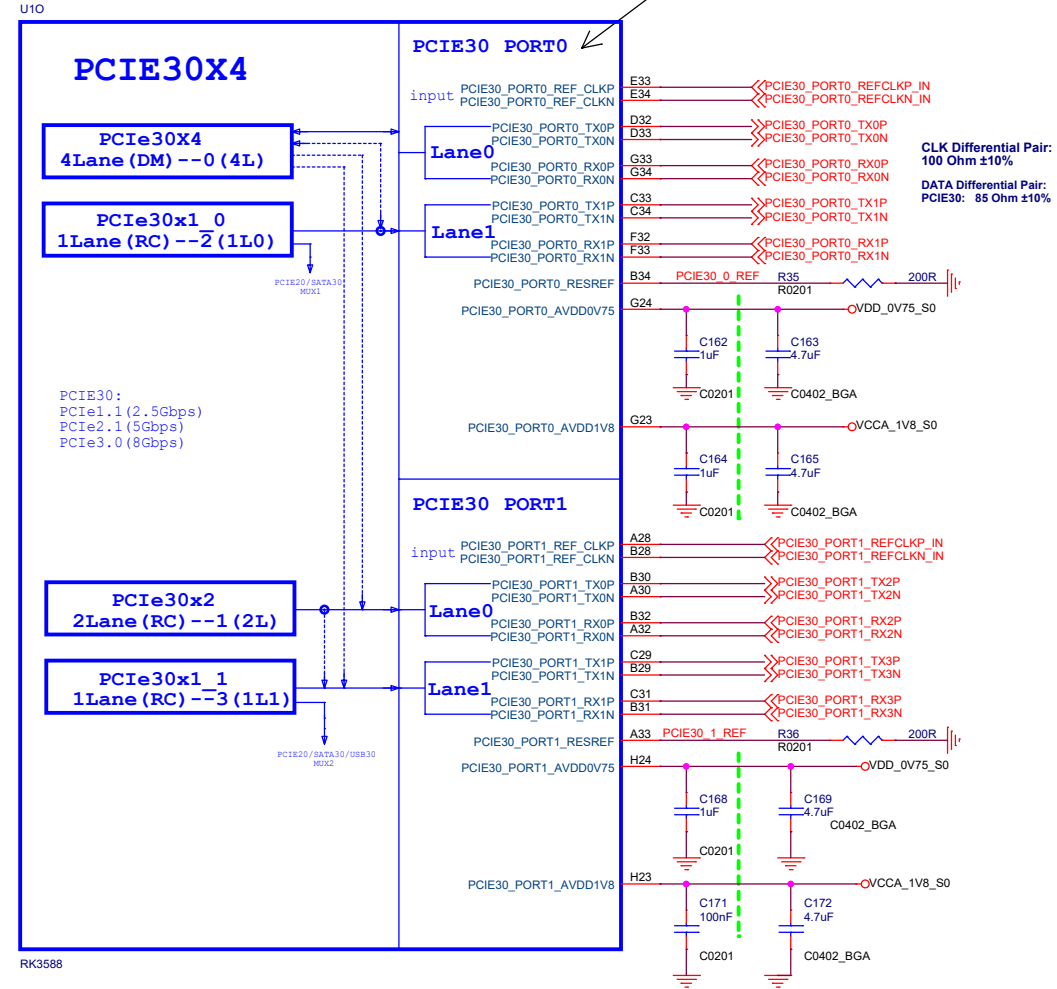
RK3588_N(PCIe20)



Note:
The SATA differential trace impedance is 100 OHM
The SATA trace length is less than 5 inch

Note:
If not used:
Signal:leave floating
Power: Floating

RK3588_O(PCIe30)



Note:
If Port0 and Port1 are not used,
Port0 and Port1 REF_CLKP/N: Leave floating or tie to VSS
Port0 and Port1 Other Signal: Leave floating
Port0 and Port1 Power: Leave floating or tie to VSS

If Port0 is used ,Port1 is not used,
Port1 REF_CLKP/N: Leave floating or tie to VSS
Port1 Other Signal: Leave floating
Port1 Power: Must supply power

If Port1 is used ,Port0 is not used,
Port0 REF_CLKP/N: Leave floating or tie to VSS
Port0 Other Signal: Leave floating
Port0 Power: Must supply power

Note:
Only PCIe3.0 Controller 0
support RC and EP,Other
controller only support RC
Mode.

VCCIO5 Domain																
Operating Voltage=1.8V/3.3V																
PM012 MD	/	SP14 MD0 MD	/	PM011 TX MD	/	I2C04 SDA MD	/	FBP01 DQ MD	/	I2D01 MDCLK	/	SDIO DQ MD	/	GMAC1 TXD2	/	GPIO3 AD MD
AUD00M MD	/	SP14 MD01 MD	/	PM011 TX MD	/	I2C04 SDA MD	/	FBP01 DQ MD	/	I2D01 MDCLK	/	SDIO DQ MD	/	GMAC1 TXD2	/	GPIO3 A1 MD
AUD00M LP	/	SP14 CLK MD	/	UART5 TX MD	/	FBP01 DQ MD	/	I2D01 MDCLK	/	SDIO DQ MD	/	SDIO DQ MD	/	GMAC1 RXD0	/	GPIO3 A2 MD
AUD00M MD	/	SP14 CSD MD	/	UART5 RX MD	/	FBP01 DQ MD	/	I2D01 MDCLK	/	SDIO DQ MD	/	SDIO DQ MD	/	GMAC1 RXD1	/	GPIO3 A3 MD
AUD00M SP	/	SP14 CBI MD	/	UART5 RSTN MD	/	/	/	I2D01 MDCLK	/	SDIO DQ MD	/	SDIO DQ MD	/	GMAC1 TXCLK	/	GPIO3 A4 MD
/	/	MIPI CAMERA0 CLK MD	/	UART5 CTEN MD	/	I2C04 SDA MD	/	FBP01 CLK MD	/	/	/	SDIO CLK MD	/	GMAC1 RXCLK	/	GPIO3 A5 MD
/	/	MIPI CAMERA0 CLK MD	/	/	/	I2C04 SCL MD	/	/	/	/	/	/	/	ETH REFCLK12M	/	GPIO3 A6 MD
PM00 MD	/	MIPI CAMERA2 CLK MD	/	/	/	/	/	/	/	/	/	/	GMAC1 RXD0	/	GPIO3 A7 MD	
PM00 MD	/	MIPI CAMERA3 CLK MD	/	/	/	/	/	/	/	/	/	/	GMAC1 RXD1	/	GPIO3 A8 MD	
/	/	MIPI CAMERA3 CLK MD	/	UART5 TX MD	/	/	/	/	/	/	/	/	GMAC1 RXD0	/	GPIO3 B1 MD	
PM01 TX MD	/	/	UART5 RX MD	/	/	/	/	I2D01 MDCLK	/	/	/	/	GMAC1 TXD0	/	GPIO3 B2 MD	
/	/	UART5 RSTN	/	/	/	/	/	I2D01 MDCLK	/	/	/	/	GMAC1 TXD1	/	GPIO3 B3 MD	
/	/	UART5 CTEN	/	/	/	/	/	I2D01 MDCLK	/	/	/	/	GMAC1 TXD2	/	GPIO3 B4 MD	
PM012 MD	/	CAN0 RX MD	/	UART5 TX MD	/	/	/	I2D01 MDCLK	/	/	/	/	GMAC1 TXD0	/	GPIO3 B5 MD	
PM013 MD	/	CAN0 TX MD	/	UART5 RX MD	/	/	/	I2D01 MDCLK	/	/	/	/	GMAC1 TXD1	/	GPIO3 B6 MD	
/	/	/	/	/	/	I2C03 SCL MD	/	SP11 MD01 MD	/	MD00 TX0 SDA MD	/	/	GMAC1 MC1W00T	/	GPIO3 B7 MD	
/	/	UART5 TX MD	/	/	/	I2C03 SDA MD	/	SP11 MD01 MD	/	MD00 TX0 SDA MD	/	/	GMAC1 PPR010	/	GPIO3 C0 MD	
/	/	PCIE0004 BUTTON RSTN	/	/	/	/	/	/	/	/	/	/	GMAC1 PPR010	/	GPIO3 C1 MD	
PM014 MD	/	/	UART5 RSTN MD	/	I2C04 SCL MD	/	SP11 CSD MD	/	/	/	MIPI TX0	/	GMAC1 MD0	/	GPIO3 C2 MD	
CAN0 RX MD	/	PCIE0004 CLAREN0 MD	/	UART5 TX MD	/	FBP01 CSD MD	/	SP13 CSD MD	/	MD00 TX1 CLK MD	/	/	CIF D0	/	GPIO3 C3 MD	
CAN0 TX MD	/	PCIE0004 WAKEN MD	/	UART5 RX MD	/	FBP01 CSD MD	/	SP13 CSD MD	/	MD00 TX1 CLK MD	/	/	CIF D0	/	GPIO3 C4 MD	
/	/	PCIE0004 WAKEN MD	/	UART5 RX MD	/	FBP01 CSD MD	/	SP13 CSD MD	/	MD00 TX1 CLK MD	/	/	CIF D0	/	GPIO3 C5 MD	
/	/	PCIE0004 PERSTN MD	/	/	/	SP13 MD01 MD	/	MD00 TX0 SCL MD	/	/	/	CIF D10	/	GPIO3 C6 MD		
/	/	PCIE0001 2 CLAREN0 MD	/	/	/	I2C03 SCL MD	/	SP13 MD01 MD	/	MD00 TX0 SCL MD	/	/	CIF D11	/	GPIO3 C7 MD	
PM00 MD	/	PCIE0001 2 WAKEN MD	/	UART5 RX MD	/	/	/	SP13 CLK MD	/	MD00 TX0 SDA MD	/	/	CIF D12	/	GPIO3 D0 MD	
/	/	PCIE0001 2 PERSTN MD	/	/	/	/	/	SP13 CLK MD	/	MD00 TX0 SDA MD	/	/	CIF D13	/	GPIO3 D1 MD	
/	/	PCIE0004 CLAREN0 MD	/	UART5 RSTN MD	/	SP11 MD01 MD	/	MD00 RX SCL MD	/	/	/	CIF D14	/	GPIO3 D2 MD		
PM01 MD	/	PCIE0004 WAKEN MD	/	UART5 CTEN MD	/	I2C07 SDA MD	/	SP10 CLK MD	/	MD00 RX SDA MD	/	/	CIF D15	/	GPIO3 D3 MD	
/	/	PCIE0004 PERSTN MD	/	UART5 RX MD	/	/	/	SP10 CSD MD	/	MD00 RX RSTP00T MD	/					

VCCIO6 Domain
Operating Voltage=1.8V/3.3V

Pin	Function	Pin	Function	Pin	Function	Pin	Function
SP10_WSD0_M0	/ UART5_RTSB_M0	/ I2S1_MCLK_M0	/ PCIEIOX1_4_CLKREQB_M0	/ BT1120_D0	/ C1F_D0	/ GPIO4_A0_d	AK30
SP10_WSD1_M0	/ UART5_CTSB_M0	/ I2S1_SCLK_M0	/ PCIEIOX1_1_WAKEN_M0	/ BT1120_D1	/ C1F_D1	/ GPIO4_A1_d	AL30
SP10_CLK_M0	/	/ I2S1_LCKM_M0	/ PCIEIOX1_3_PERSTB_M0	/ BT1120_D2	/ C1F_D2	/ GPIO4_A2_d	AM29
UART0_TX_M2	/	/	/ PCIEIOX1_5_CLKREQB_M0	/ BT1120_D3	/ C1F_D3	/ GPIO4_A3_d	AL28
SP12_WSD0_M0	/ UART0_RX_M2	/ I2C3_SCL_M2	/ PCIEIOX1_0_WAKEN_M0	/ BT1120_D4	/ C1F_D4	/ GPIO4_A4_d	AL29
SP12_WSD1_M0	/ UART3_TX_M2	/ I2C3_SDA_M2	/ PCIEIOX1_6_PERSTB_M0	/ BT1120_D5	/ C1F_D5	/ GPIO4_A5_d	AL27
SP12_CLK_M0	/ UART3_RX_M2	/ I2C5_SCL_M2	/ I2S1_B0TB_M0	/	/	/ GPIO4_A6_d	AL72
SP12_CSD0_M0	/	/ I2S1_B0TB_M0	/ PCIEIOX2_CLKREQB_M0	/ BT1120_D6	/ C1F_D6	/ GPIO4_A6_d	AM27
SP12_CSD1_M0	/	/ I2S1_B0TB_M0	/ PCIEIOX2_WAKEN_M0	/ BT1120_D7	/ C1F_D7	/ GPIO4_A7_d	AK28
SP12_CSD2_M0	/	/ I2S1_B0TB_M0	/ PCIEIOX2_PERSTB_M0	/ BT1120_CLKOUT	/ C1F_CLKIN	/ GPIO4_B0_d	AL26
DATAX_ACT_LED_M0	/ SPDIF1_TX_M1	/ SP10_CSD1_M0	/ I2S1_B0TB_M0	/ PCIEIOX1_0_BUTTON_RSTB	/	/ MIPI_CAMERA0_CLK_M0	AL24
CAN1_RX_M1	/ RMW1_M1	SP10_CSD0_M0	/ I2C3_SCL_M3	/ I2S1_B0TB_M0	/ C1F_HREF	/ GPIO4_B1_d	AK25
CAN1_TX_M1	/ RMW1_TX_M1	/	/	/ I2S1_B0TB_M0	/ PCIEIOX1_2_BUTTON_RSTB	/ BT1120_D8	/ C1F_VSYNC
SP1F0_TX_M1	/ RMW1_TX_M1	/ DPO_RPDIN_M0	/ UART5_TX_M1	/ I2S1_B0TB_M0	/ PCIEIOX3_CLKREQB_M0	/	AL26
DATAL_ACT_LED_M0	/ RMW02_M0	SP12_WSD0_M0	/ UART5_RX_M0	/	/	/	AL27
/	/	SP12_CSD1_M0	/	/ I2S1_B0TB_M0	/ PCIEIOX4_WAKEN_M0	/	AL28
/	/	SP12_CSD2_M0	/	/ I2S1_B0TB_M0	/ PCIEIOX1_2_CLKREQB_M0	/ BT1120_D13	/
/	/	SP12_CSD3_M0	/	/ I2S1_B0TB_M0	/ PCIEIOX1_1_WAKEN_M0	/ BT1120_D14	/
SPDIF1_TX_M2	/ RMW6_M1	SP12_CSD1_M0	/ I2C3_SCL_M3	/ DM12_TX0_CEC_M0	/ PCIEIOX1_3_PERSTB_M0	/ BT1120_D15	/

Physical Pin Layout (Left side):

- AK30, AL30, AM29, AL28, AL29, AL27, AL72, AK28, AL26, AL24, AK25, AL26, AL27, AL28, AL29, AK24

Physical Pin Layout (Right side):

- CNC_V1B_90, C174 100nf, C0001, CNC_3V3_90, C175 100nf, C0001

VCCIO4 Domain		Operating Voltage=1.8V/3.3V	
/BP14 MISO_M2 / PCIE3IOX1_1_CLKREQ_M2 / SPO_RPDSN_M2	/I2C2_SDA_M4 / UART6_RX_M1 / GPIO1_A0_0	A24	>>BP14_MISO_M2
BATA1_ACT_LED_M1 /	/	A25	>>BP14_MOSI_M2
/PWRM0_M2 / BP14_CLK_M2 /	/VOP_POST_ENPTT / I2C4_SDA_M3 / UART6_RTSN_M1 / GPIO1_A2_0	A26	>>BP14_CLK_M2
/PWRM1_M2 / BP14_CS0_M2 /	/RDGN_TX1_SDA_M2 / I2C4_SCL_M3 / UART6_CTSN_M1 / GPIO1_A3_0	A27	>>BP14_CS0_M2
/BP12 MISO_M0 /	/RDGN_TX1_SCL_M2 /	B25	>>GPIO1_A4
/	/BP12 MOSI_M0 /	B26	<<HDMITX_HPDSN_M0
/BP12_CLK_M0 /	/RDGN_TX1_HPD_M0 /	C24	>>PWRDIS
/	/	C25	
/BP12_CS1_M0 / PCIE3IOX4_CLKREQ_M3 /	/PDM1_SDI1_M3 /	C27	>>ACTIVITY#
/BP10 MISO_M2 / PCIE3IOX4_WAKEN_M3 /	/PDM1_SDI2_M3 /	D25	>>IDIR
/BP10 MOSI_M2 / PCIE3IOX4_PERRSTN_M3 /	/PDM1_SDI3_M3 / UART4_RX_M2 / GPIO1_B2_4	D26	<<PCIE30_PWRFN_H
BATA2_ACT_LED_M1 /	/PDM1_CLK1_M3 / UART4_TX_M2 / GPIO1_B3_4	D27	>>PCIE1_0_WAKEN_M2
/BP10_CLK_M2 / PCIE3IOX1_0_WAKEN_M2 /	/PDM1_CS0_M3 /	E24	>>PCIE1_0_PERRSTN_M2
/	/BP10_CS1_M2 / PCIE3IOX1_0_CLKREQ_M2 /	E25	>>PCIE1_0_CLKREQ_M2
/RDGN_RX_RPODST_M2 /	/SPOIFL_TX_M0 / RDGN_TX1_SCL_M2 / I2C9_SCL_M3 / UART1_TX_M1 / GPIO1_B6_U	E26	<<I2CS_SDA_M3
BATA2_ACT_LED_M1 / RDGN_RX_CS0_M2 / PWRM1_M2	/SPOIFL_TX_M0 / PCIE3IOX2_PERRSTN_M3 / WPIF_CAMERA3_CLK_M0 / I2C9_SDA_M3 / UART1_RX_M1 / GPIO1_B7_U	E27	>>I2CS_SCL_M3
/RDGN_RX_SCL_M2 / PWRM0_M2 /	/	F24	>>PWRM1
/RDGN_RX_SDA_M2 / PWRM1_2B_M3 /	/PCIE3IOX2_CLKREQ_M3 / WPIF_CAMERA3_CLK_M0 / I2C9_SDA_M2 / UART1_CTSN_M1 / GPIO1_D7_U	F25	>>PWRM1
VCCIO4_V1#			
VCCIO4			

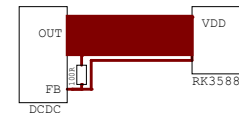
PMIC_SPI_CS
 PMIC_SPI_MOSI
 PMIC_SPI_CLK

 PMIC_PWR_CTRL1
 PMIC_PWR_CTRL2
 PMIC_PWR_CTRL3

 PMIC_INT_L

 RESET_L

 PMIC_EXT_EN_OUT



IF This device must be mounted. Replacing TVS mode is not recommended, if must, please choose the same specifications

Operating Supply Voltage: 5.5V(5.25-6V)

Peak Pulse Current: >10A (tp=8/20uS)

Surge Clamping Voltage: <6.5V

DO NOT DELETE IT!

The schematic diagram illustrates the power management section of the X93B51-QFN68, featuring a U2B power management block and various voltage regulators. The diagram is organized into two main sections: the left side shows the input and output connections for the regulators, and the right side shows the output voltages and decoupling capacitors.

Left Side (Inputs and Outputs):

- VCC_2V0_PLDO_S3:** Input to VCC11 (59) and VCC12 (64). Output to PLDO1 (59) and PLDO2 (58).
- VCC4V0_SYS:** Input to VCC12 (64).
- VCC_1V1_NLDO_S3:** Input to VCC13 (13).
- VCC_1V1_NLDO_S3:** Input to VCC14 (9).

Right Side (Outputs and Decoupling Capacitors):

- VCC11 (59):** Output to PLDO1 (59) and PLDO2 (58). Default: 1.8V.
- VCC12 (64):** Output to PLDO3 (57) and PLDO4 (63). Default: 1.8V.
- VCC13 (13):** Output to NLDO1 (14) and NLDO2 (12). Default: 1.2V.
- VCC14 (9):** Output to NLDO3 (11) and NLDO4 (10). Default: 3.3V.

Decoupling Capacitors and Default Voltages:

- C228 (1uF):** Connected to VCC11 (59). Default: 1.8V.
- C232 (1uF):** Connected to VCC12 (64). Default: 1.8V.
- C230 (1uF):** Connected to VCC13 (13). Default: 1.2V.
- C233 (1uF):** Connected to VCC14 (9). Default: 3.3V.
- C235 (1uF):** Connected to VCC15 (65). Default: 3.3V.
- C238 (2.2uF):** Connected to VDD_0V75_S3 (14). Default: 0.75V.
- C240 (2.2uF):** Connected to VDDA_DDR_PLL_S0 (12). Default: 0.85V; Low frequency: 0.85V-->0.75V.
- C243 (2.2uF):** Connected to VDDA_0V75_S0 (11). Default: 0.75V.
- C245 (2.2uF):** Connected to VDDA_0V85_S0 (10). Default: 0.85V.
- C247 (2.2uF):** Connected to VDD_0V75_S0 (8). Default: 0.75V.

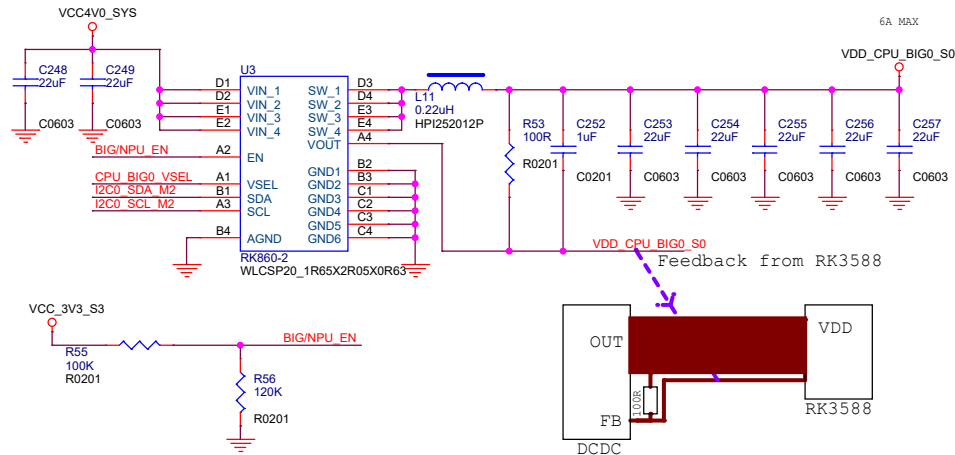
Legend:

- PLDO:** Power Load Output
- NLDO:** Non-Load Output

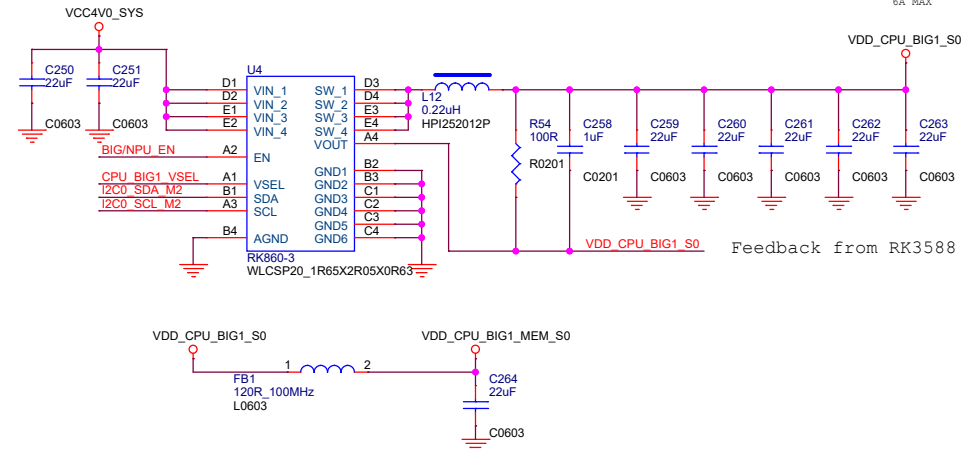
Notes:

- Default values are shown in blue.
- Low frequency: 0.85V-->0.75V is shown in red.

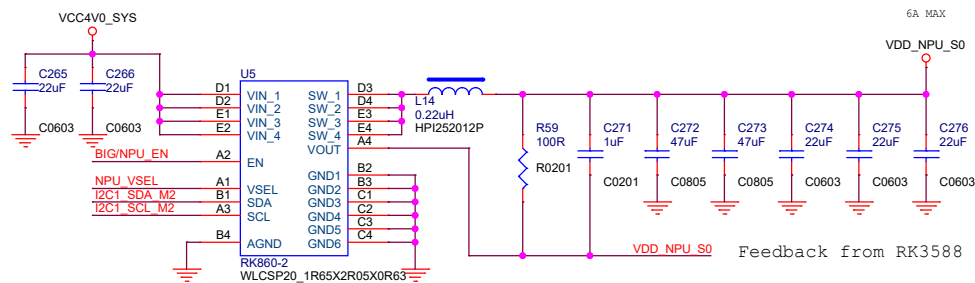
VDD_CPU_BIG0



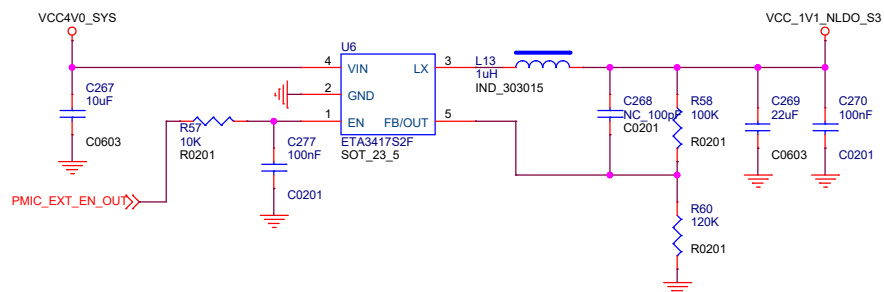
VDD_CPU_BIG1



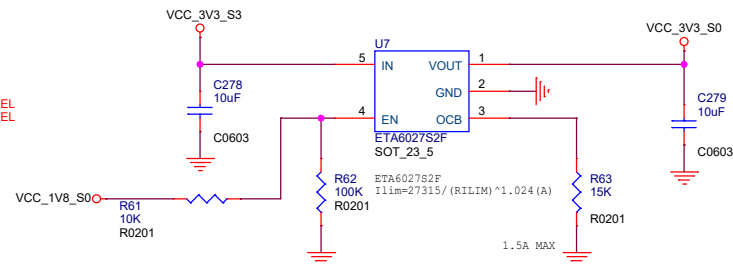
VDD_NPU



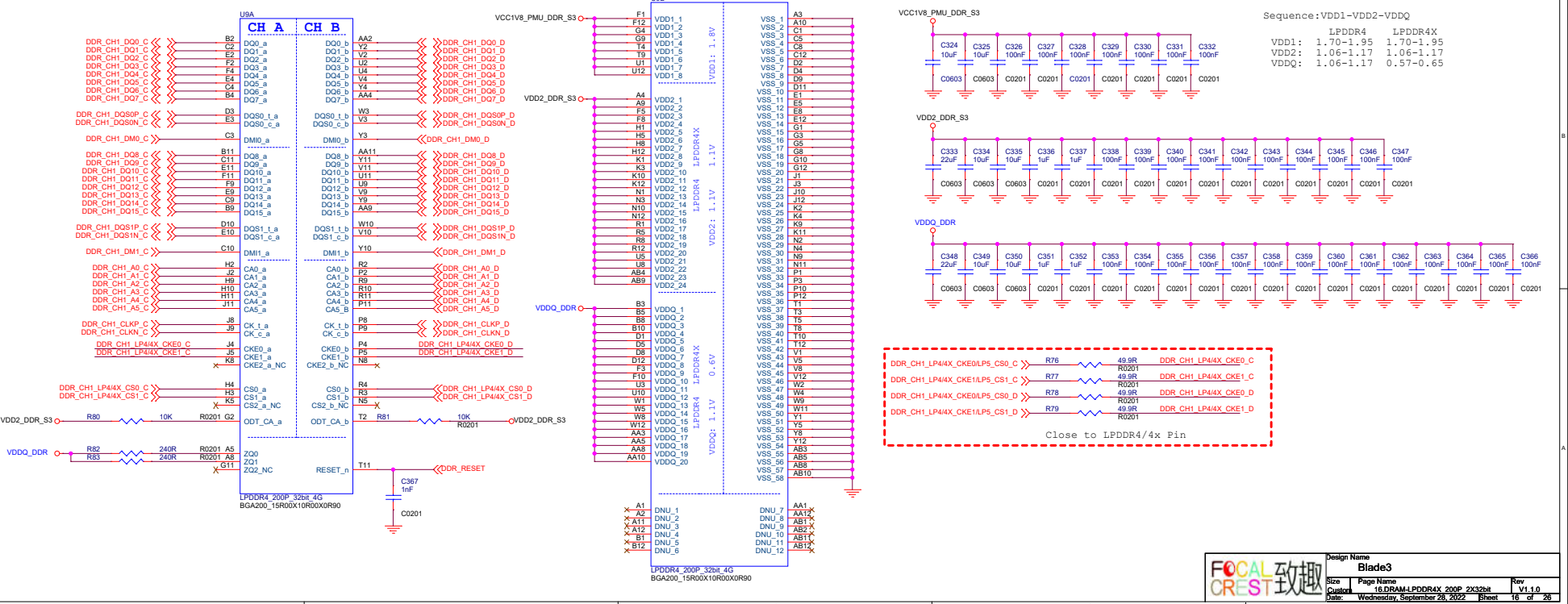
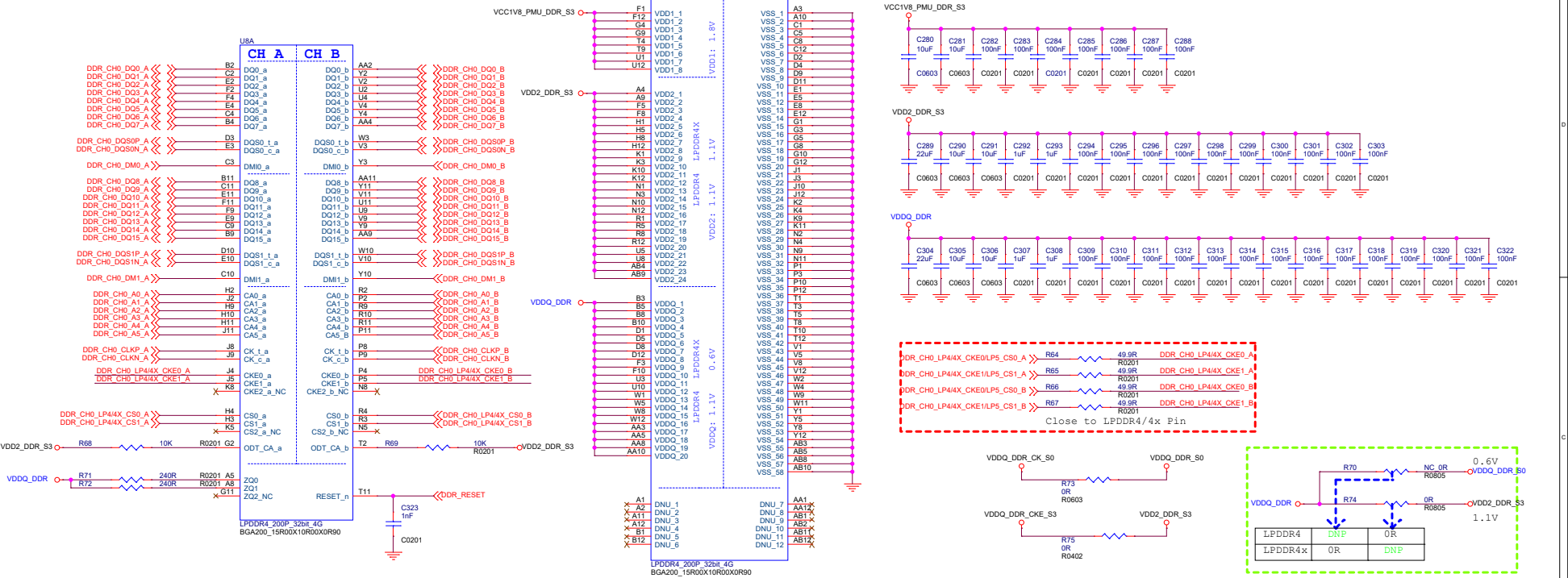
VCC_1V1_NLDO_S3



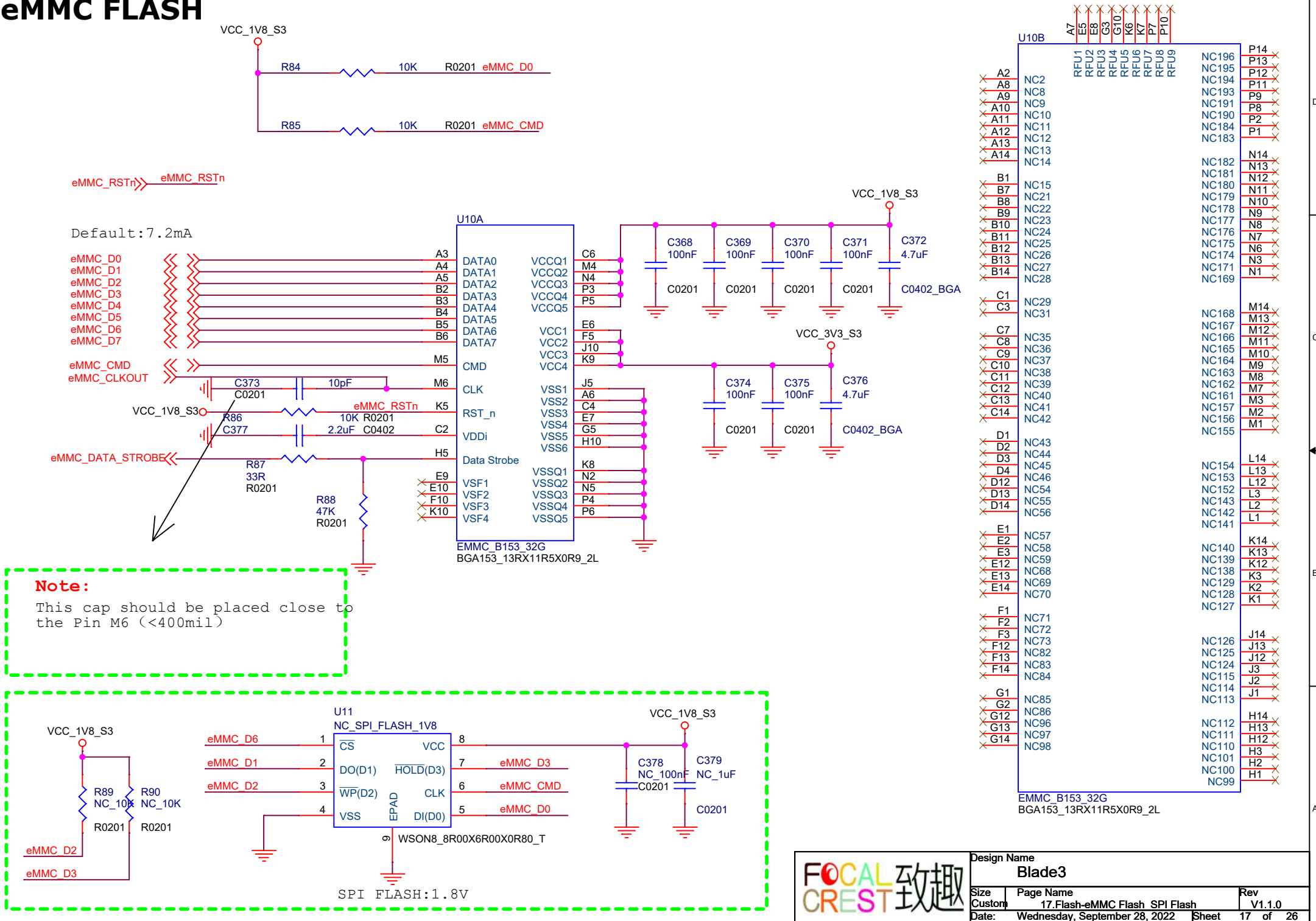
时序控制, s3为常开, s0为外设, 休眠时关闭

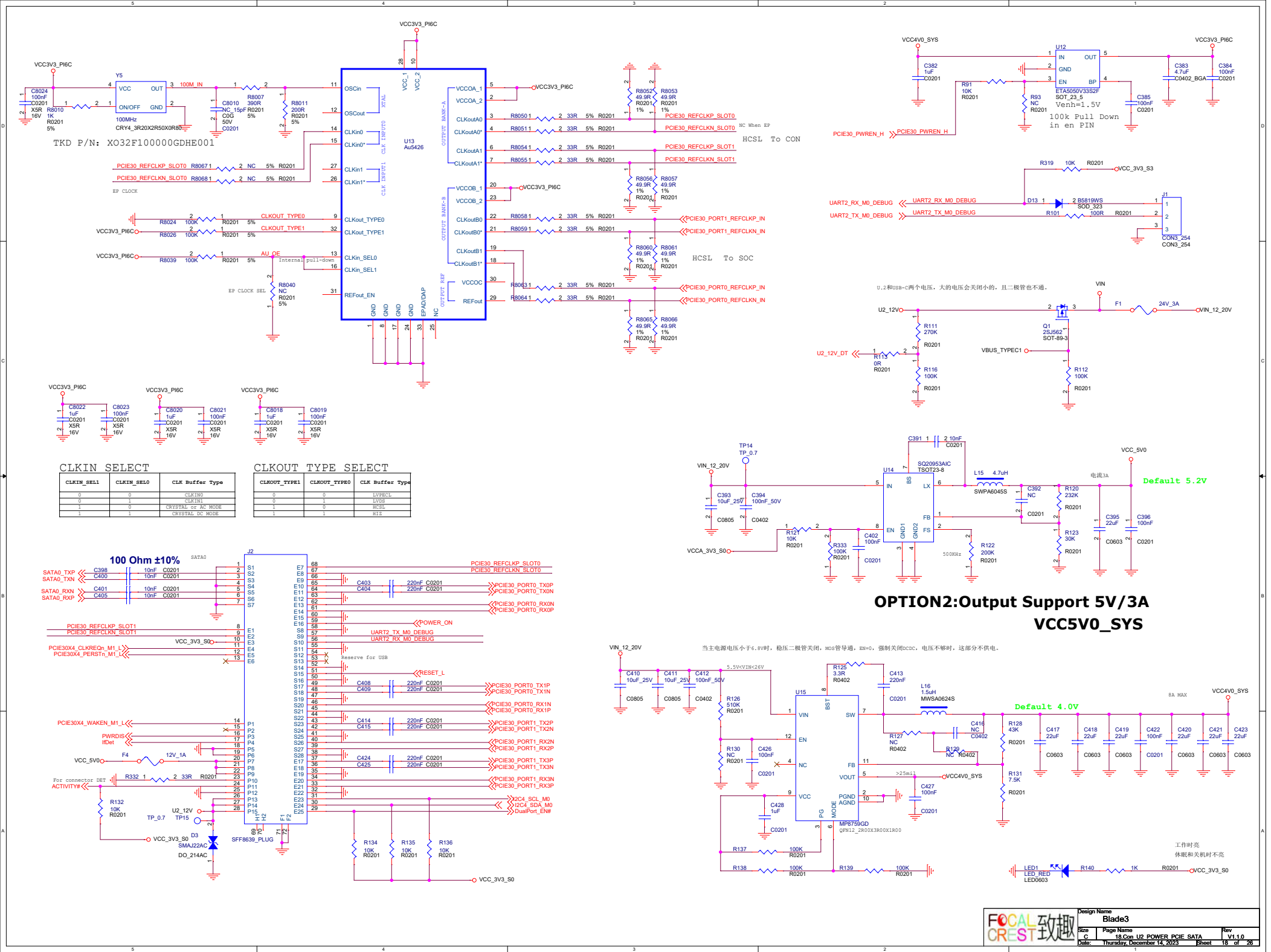


LPDDR4/4X

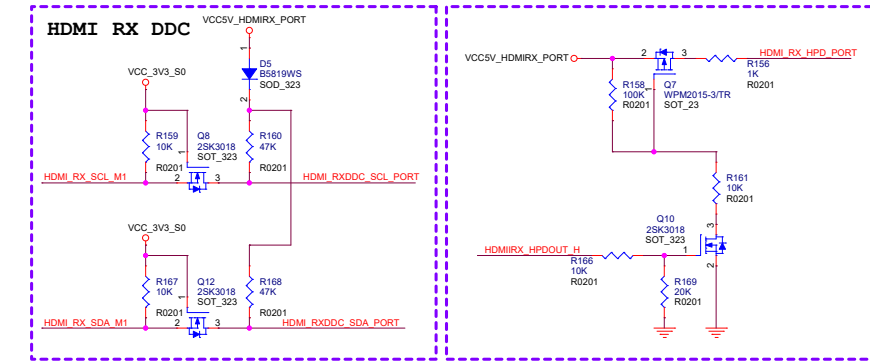
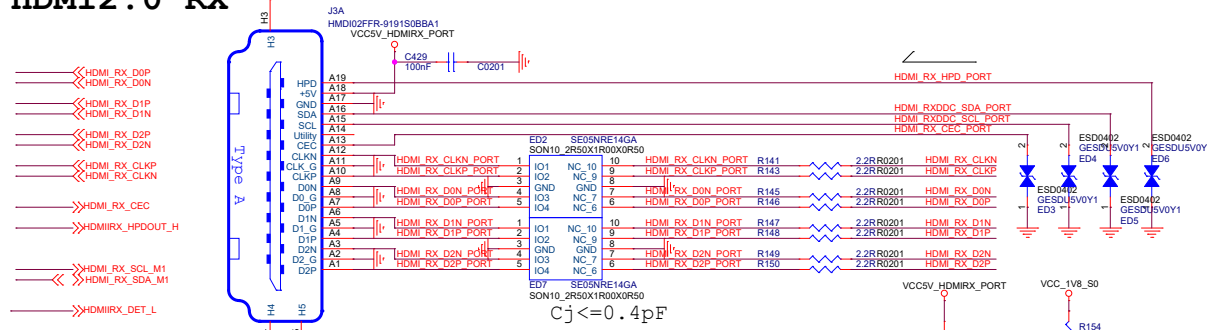


eMMC FLASH



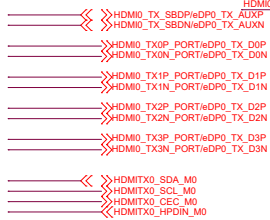


HDMI2.0 RX

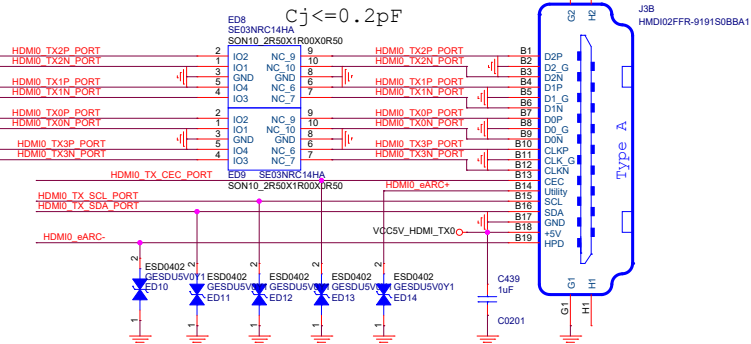
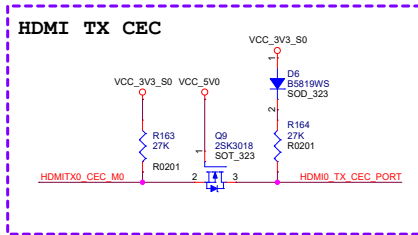
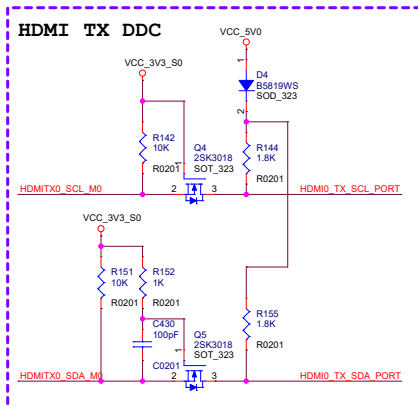
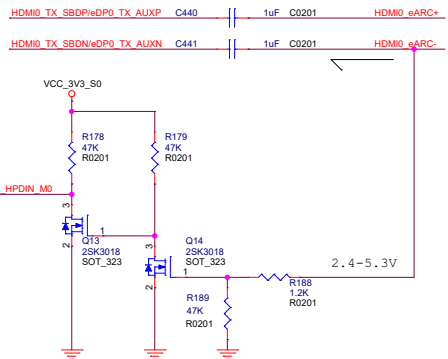


HPD: Sink Side: Require output, Min 2.4V; Max 5.3V
Source Side: Require input and Detection.
Min 2.0V; Max: 5.3V

HDMI TX0

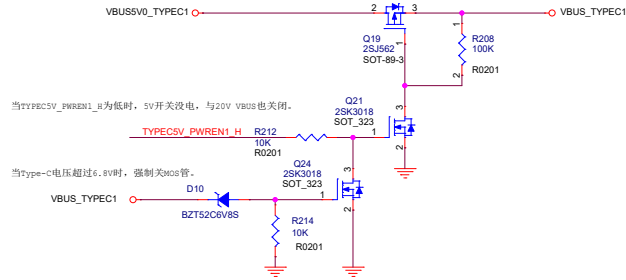
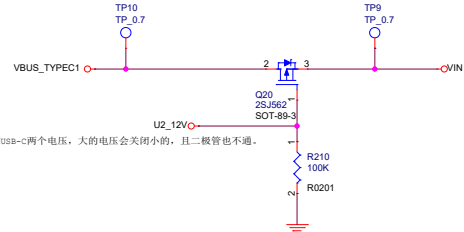
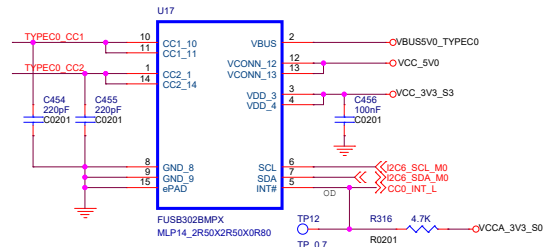
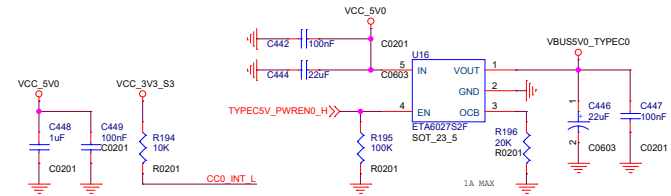
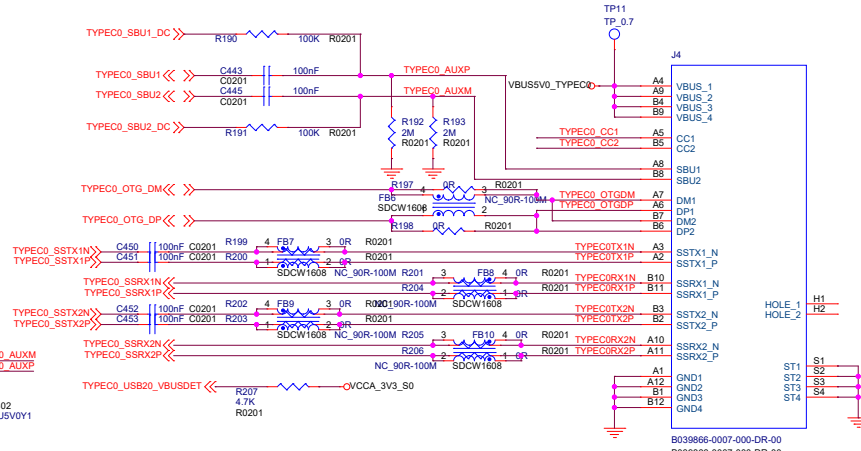
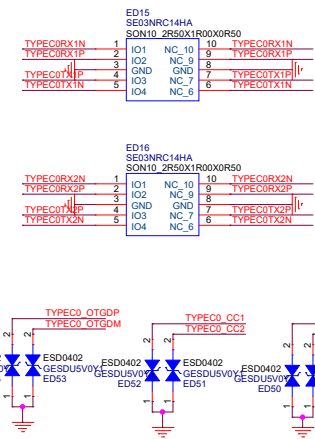


HDMI TX eARC

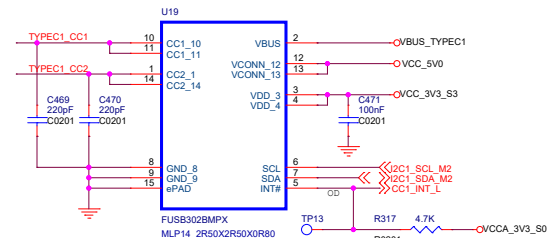
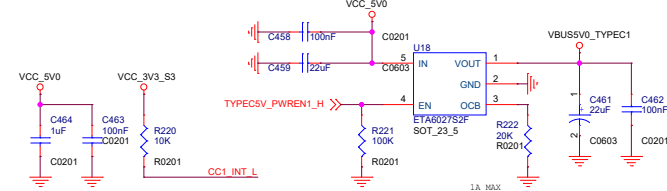
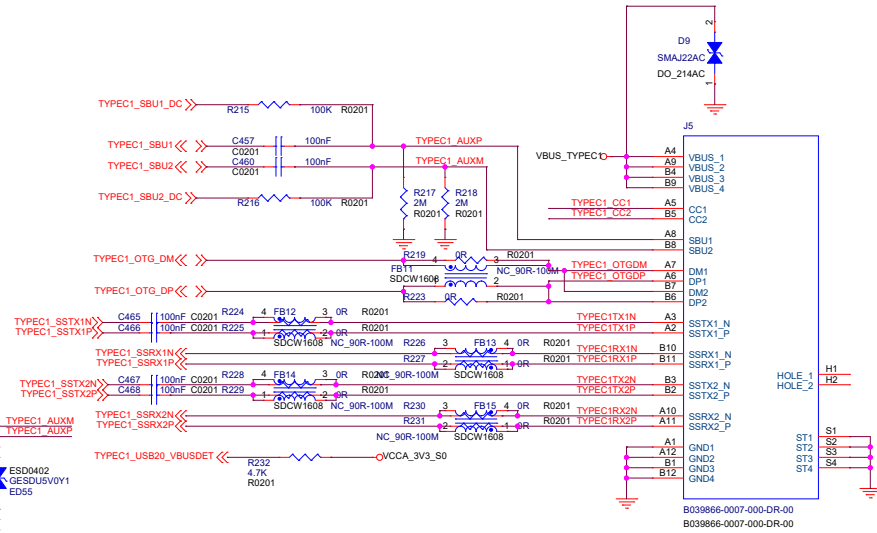
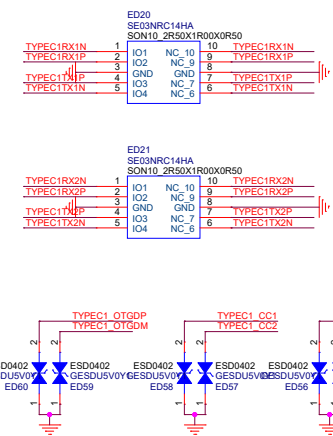


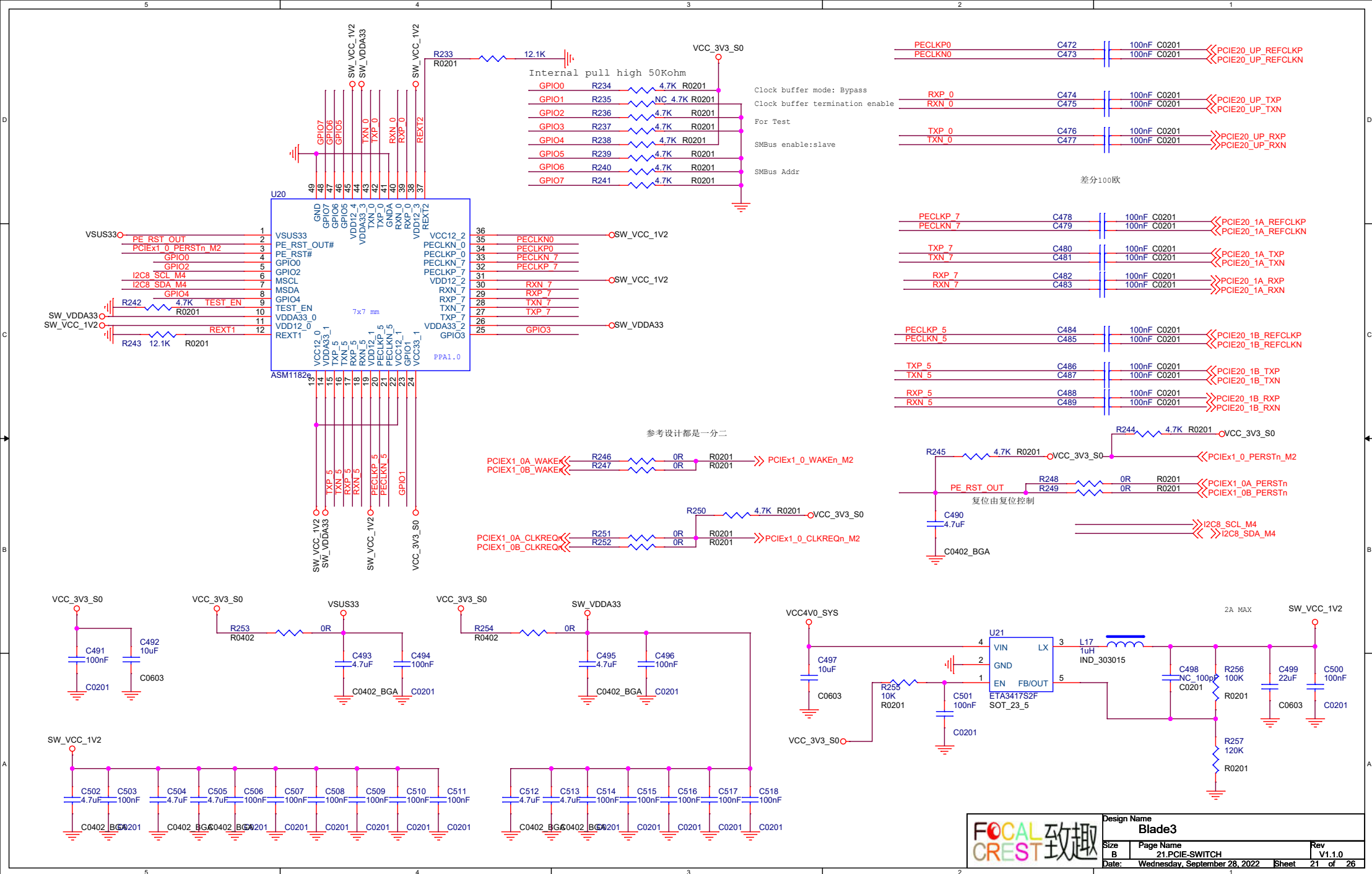
Note:
The controller only support AC coupled link in order to backward compatibility or to meet HDMI2.0 (1.4b) DC common mode spec and Voff, need do R based level-shift.
Switch on in HDMI2.0(TMDS) mode
Switch off in HDMI2.1(FRL) mode.

Type-C PORT0

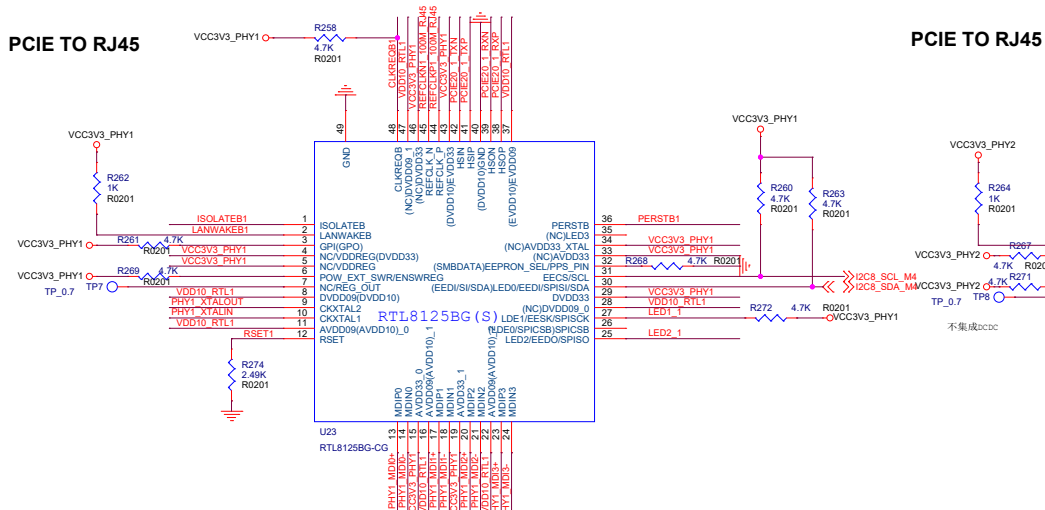


Type-C PORT1

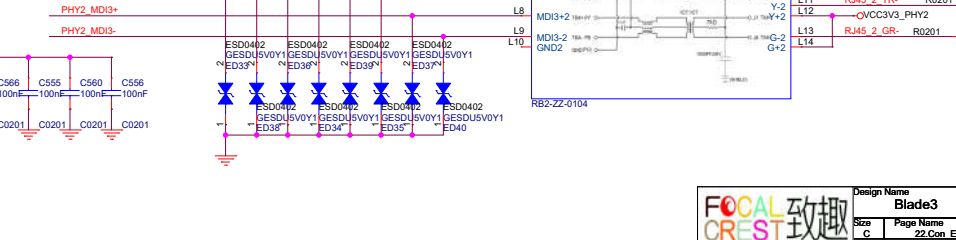
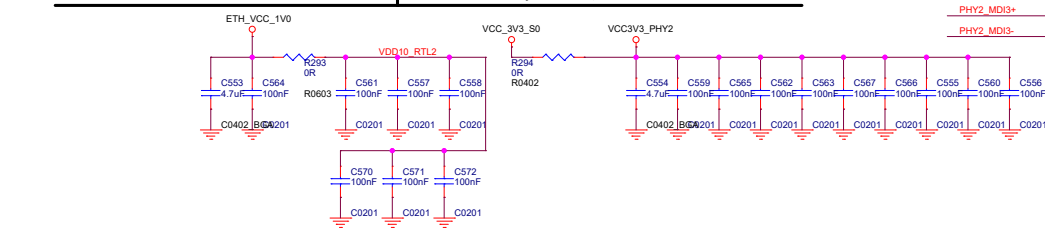
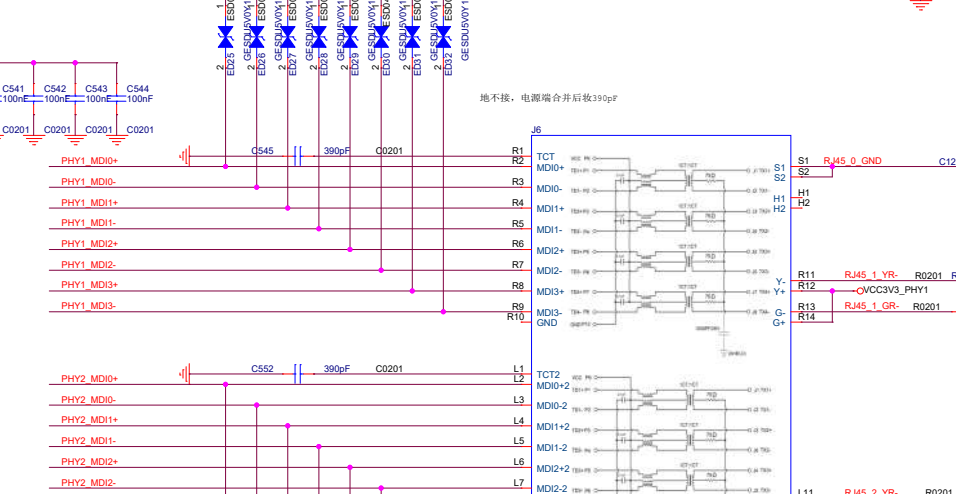
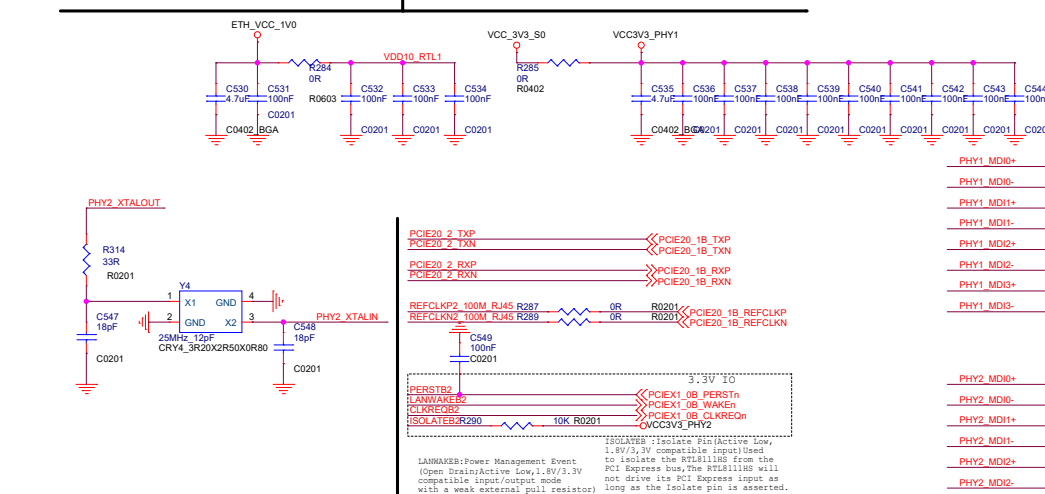
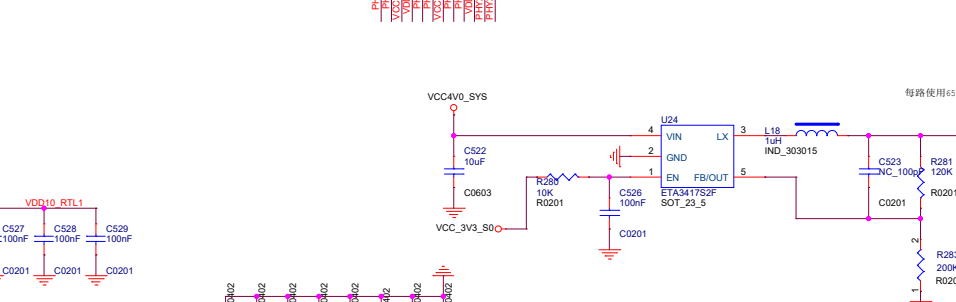
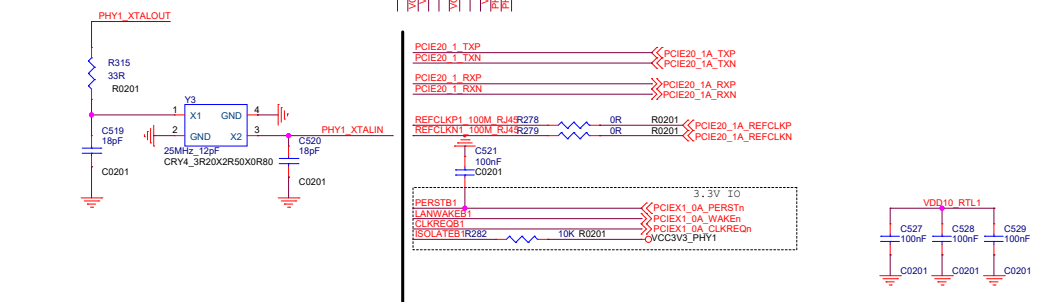
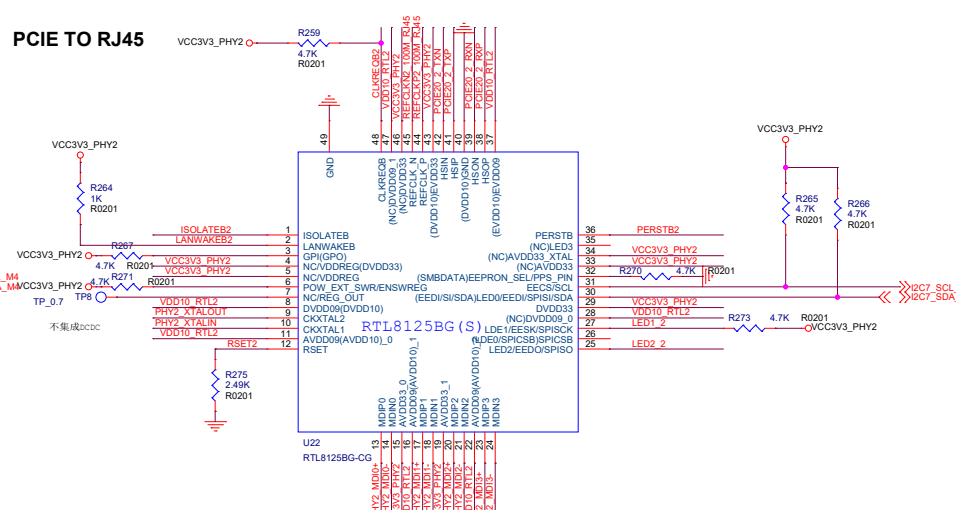


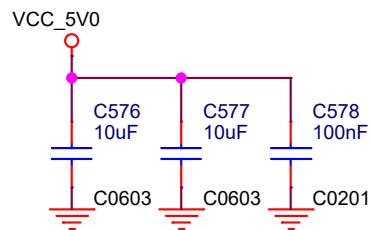
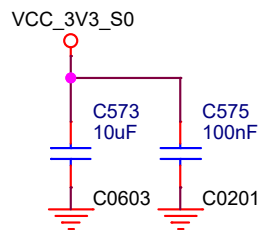


PCIE TO RJ45



PCIE TO RJ45

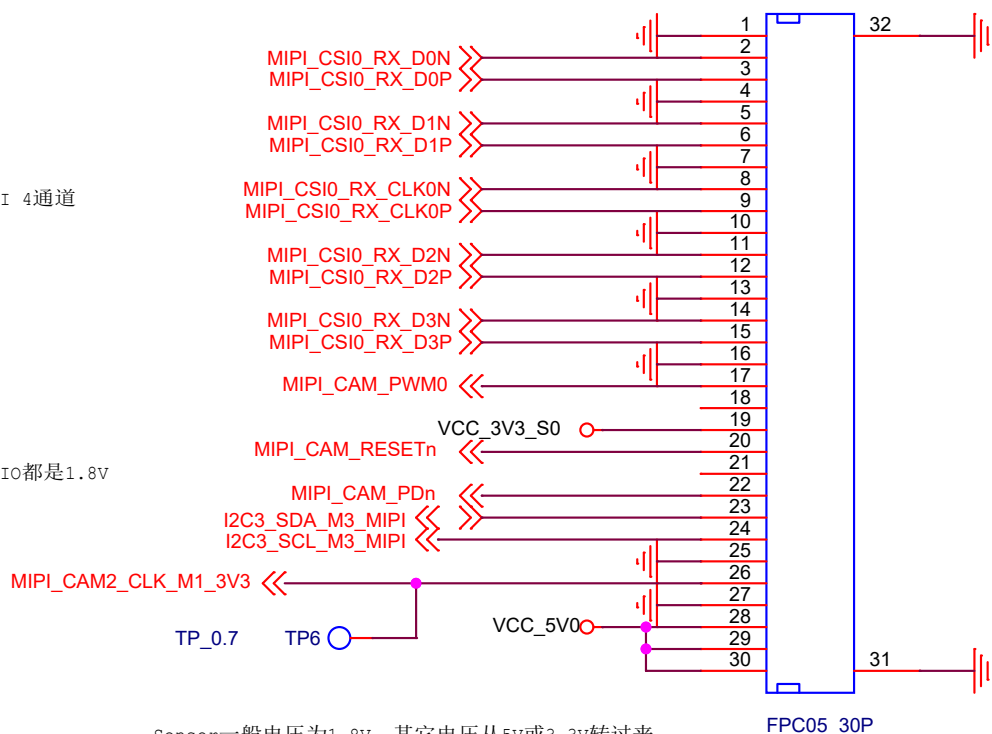




J7

CSI 4通道

这些IO都是1.8V



Sensor一般电压为1.8V，其它电压从5V或3.3V转过来

1.2V，1.8V可以用DCDC，从5V转

2.8V可以用3.3V用LDO

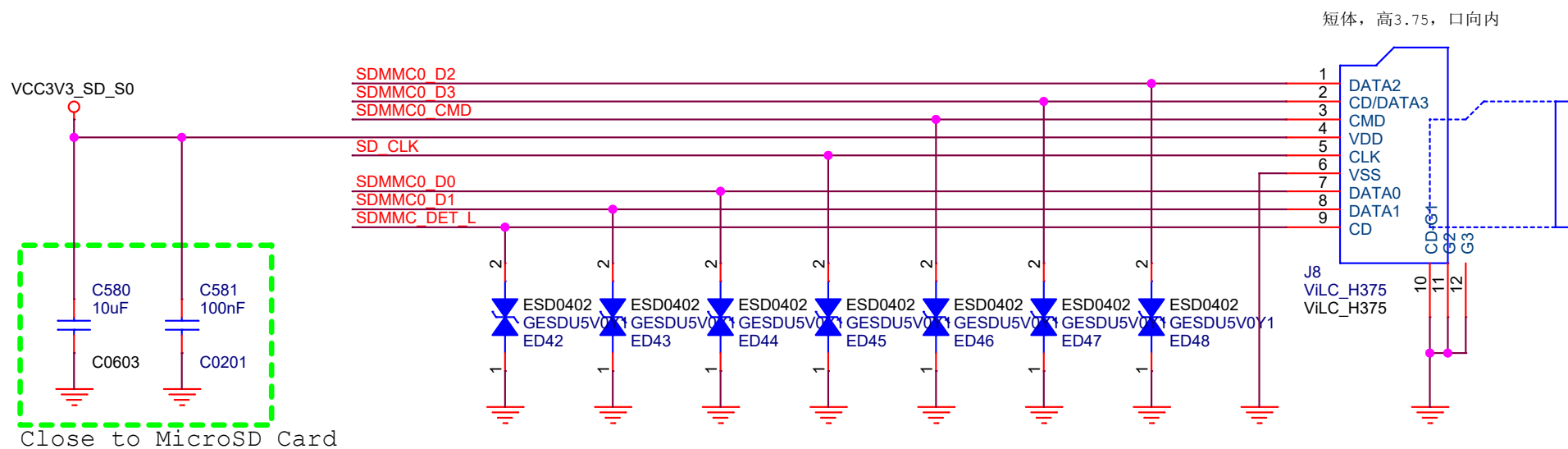
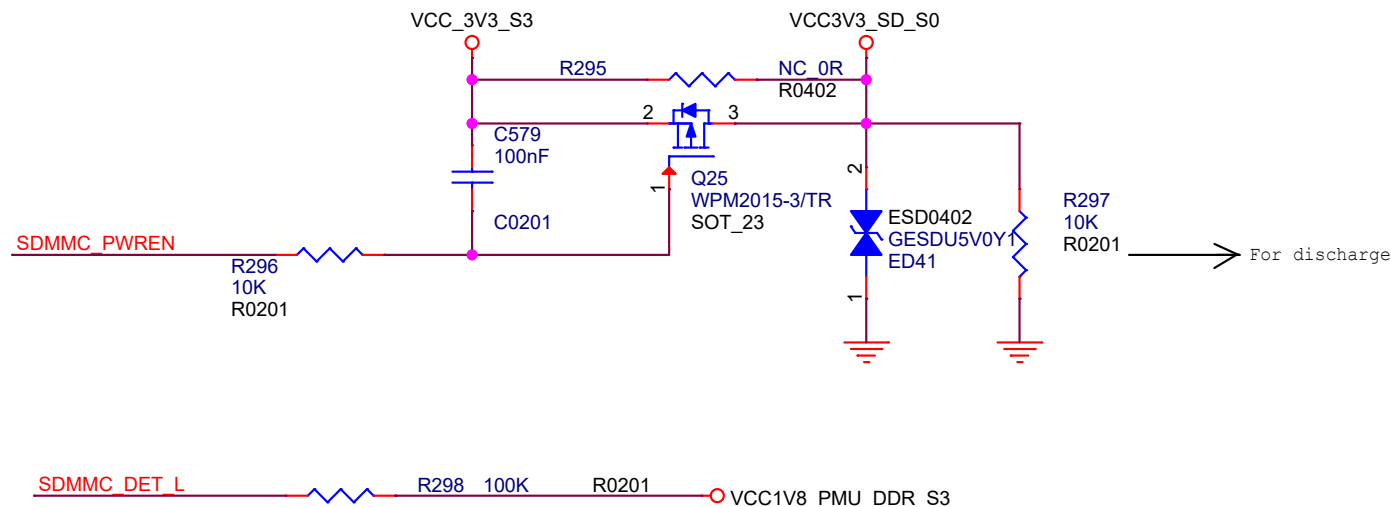
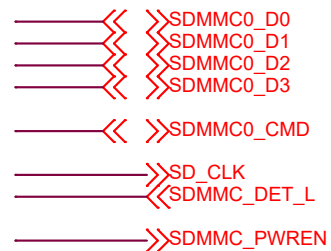
FPC Pin List

Pin1 :GND
Pin2 :D0N
Pin3 :D0P
Pin4 :GND
Pin5 :D1N
Pin6 :D1P
Pin7 :GND
Pin8 :CLKN/AUXN
Pin9 :CLKP/AUXP
Pin10:GND
Pin11:D2N
Pin12:D2P
Pin13:GND
Pin14:D3N
Pin15:D3P
Pin16:GND
Pin17:LCD_PWM_BL
Pin18:LCD_TE
Pin19:VCC3V3_LCD
Pin20:LCD_RST
Pin21:LCD_ID
Pin22:LCD_PWREN
Pin23:TP_I2C_SCL
Pin24:TP_I2C_SDA
Pin25:TP_INT
Pin26:TP_RST
Pin27:GND
Pin28:5V0
Pin29:5V0
Pin30:5V0



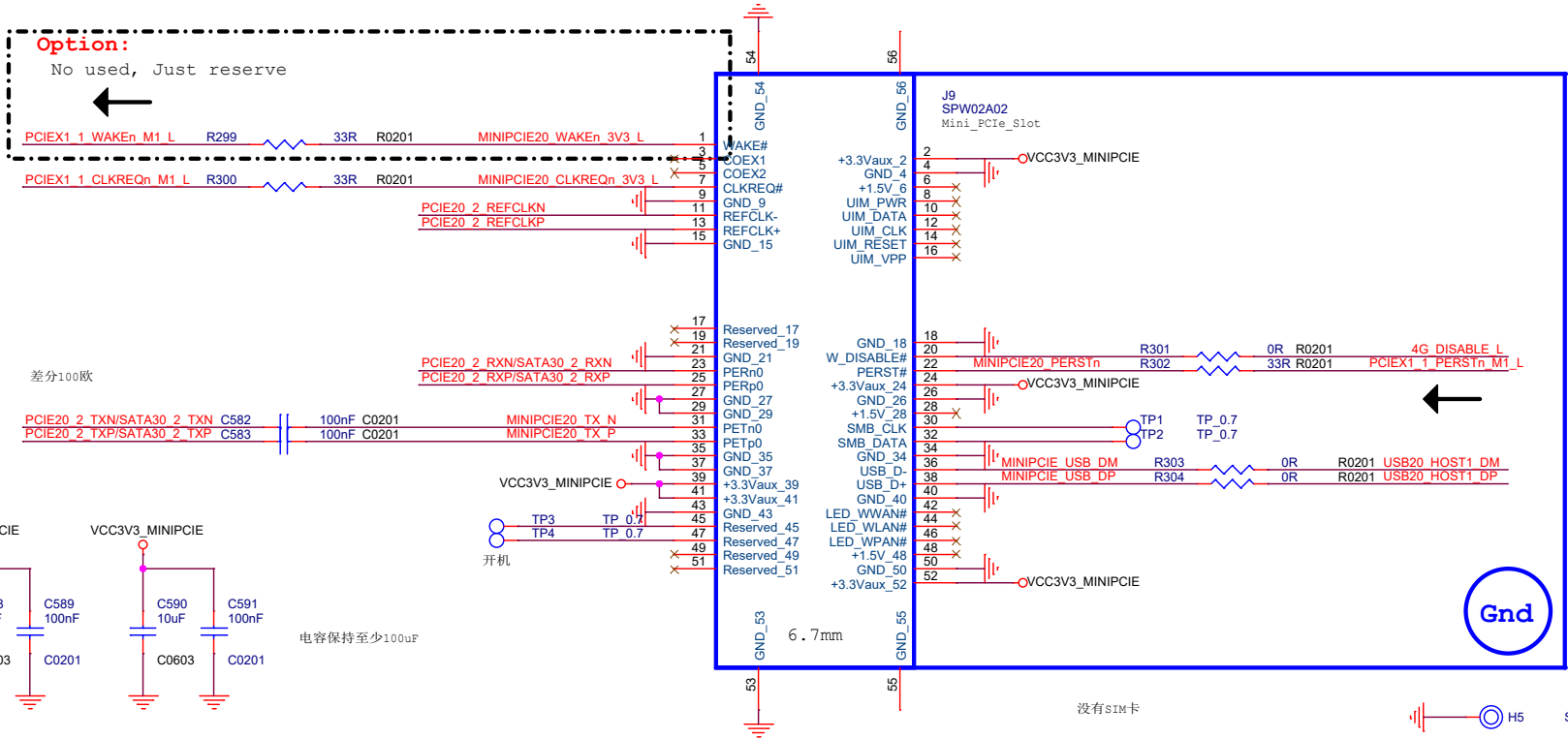
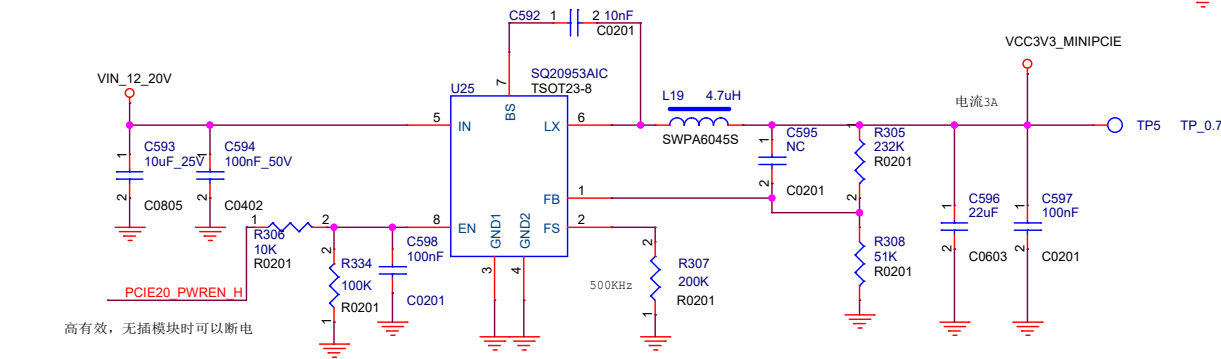
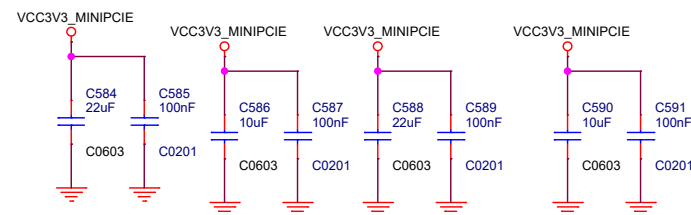
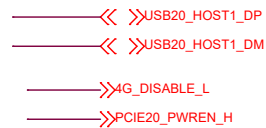
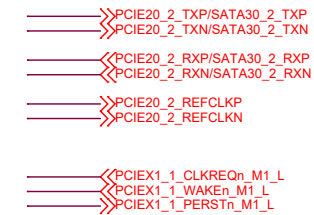
Design Name		
Blade3		
Size	Page Name	Rev
A	23.Con MIPI-DSI	V1.1.0
Date:	Wednesday, September 28, 2022	Sheet 23 of 26

TF CARD



Design Name		Blade3
Size	Page Name	Rev
A	24.Con TF Card	V1.1.0
Date:	Wednesday, September 28, 2022	Sheet 24 of 26

MiniPCIE2.0 Slot



MiniPCIE2.0 Slot Power

