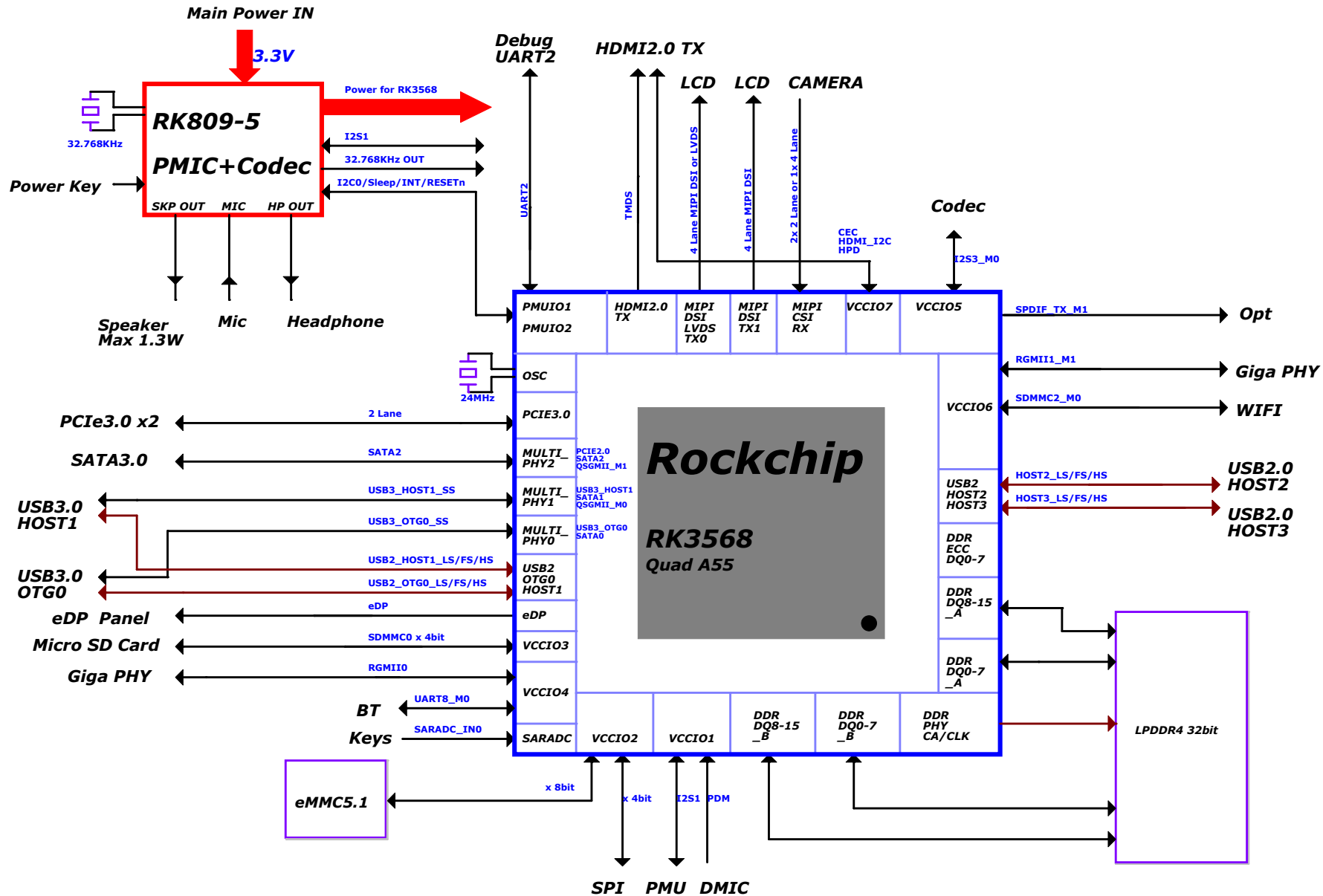


	5		4		3		2		1	
Revision History										
	Version	Date	By	Change Dscription					Approved	
D	V1.0	2021-02-02	Phi	1:Revision preliminary version						
C										
B										
A										
FOCAL CREST 致趣 Design Name Mixtile-Core-3568 Size B Page Name 01-History Date: Friday, May 06, 2022 Rev V1.2.0 Sheet 1 of 17										
	5		4		3		2		1	

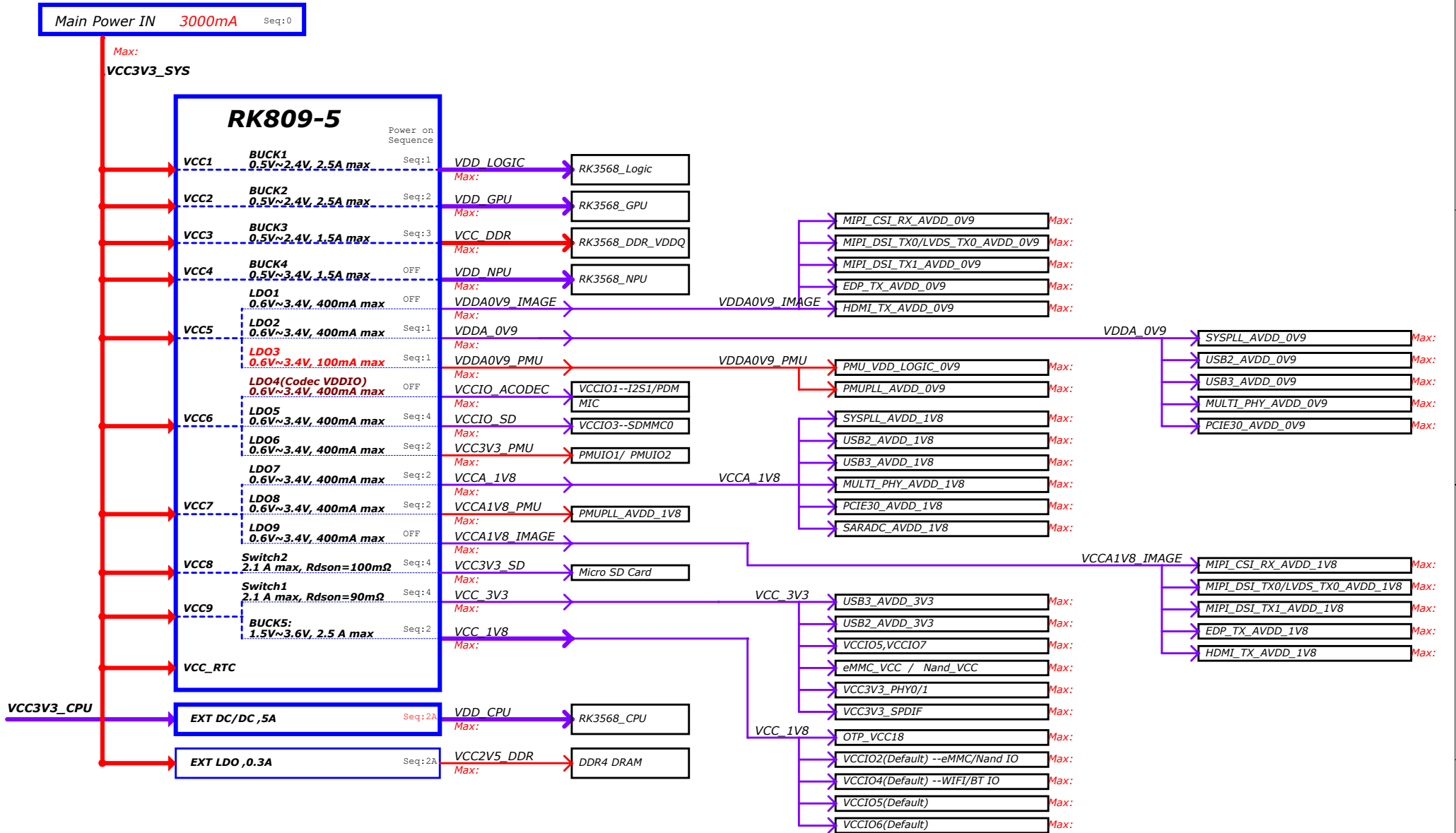
Mixtile Core RK3568



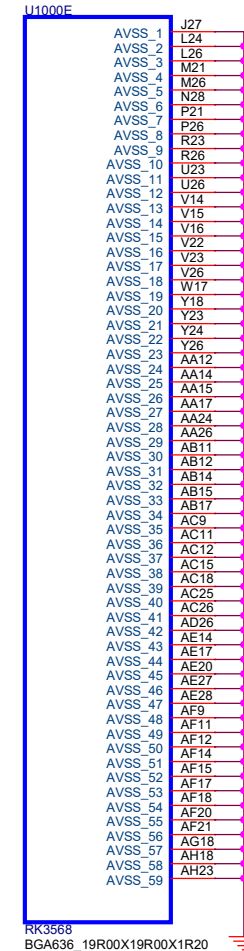
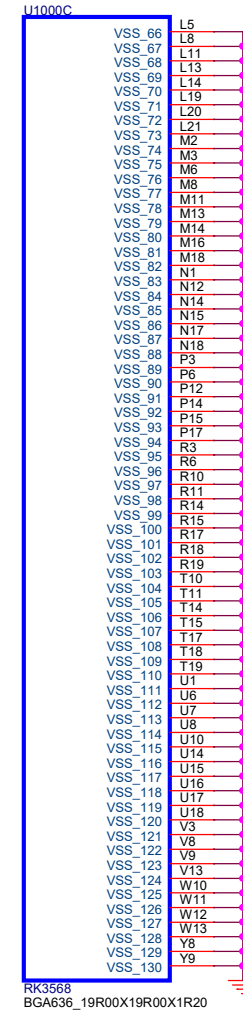
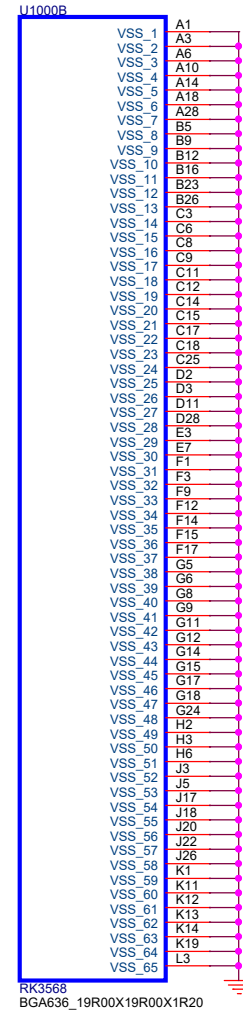
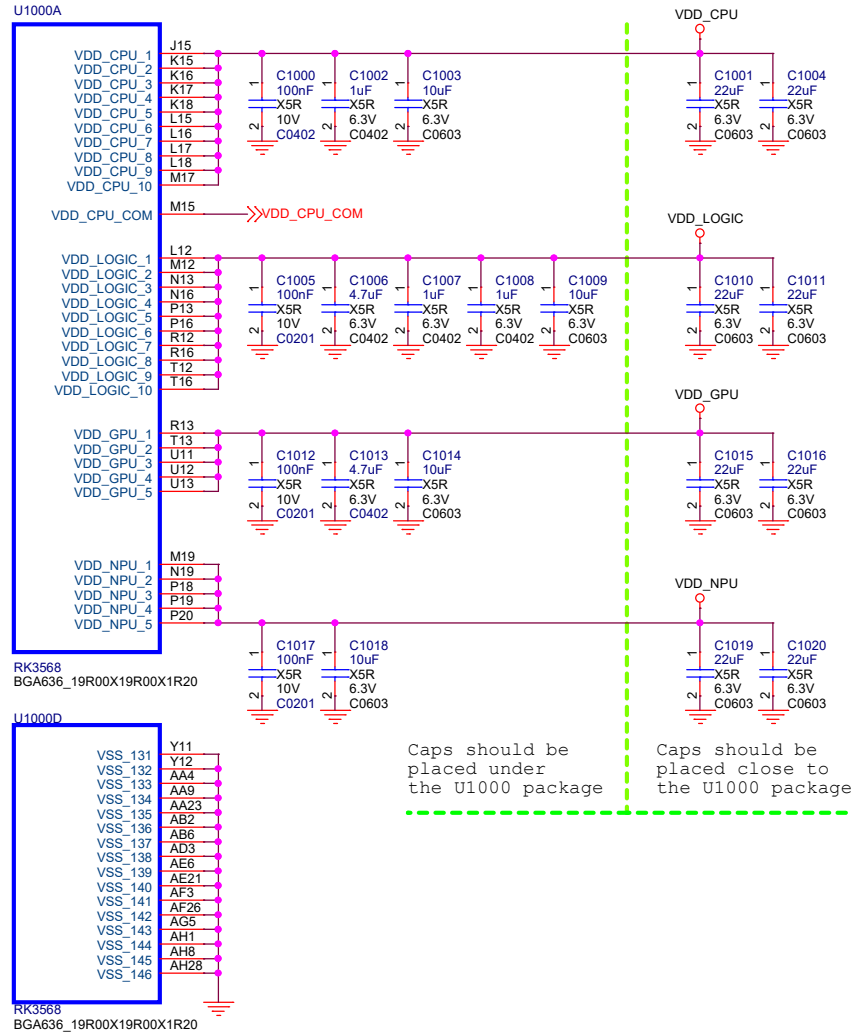
Connector

Main Power IN	Micro SD Card	Giga PHY	DMIC	Audio	Codec	GPIO
Keys	USB3.0 OTG	USB3.0/2.0 HOST	SPI	UART	I2C	WIFI
						CAMERA
						LCD
						HDMI2.0 TX

Power Diagram



RK3568_ABCDE (Power&Gnd)



U1000F

LPDDR4_DQ0_A <<> DDR DQ0_A F2
 LPDDR4_DQ1_A <<> DDR DQ1_A E1
 LPDDR4_DQ2_A <<> DDR DQ2_A E2
 LPDDR4_DQ3_A <<> DDR DQ3_A L7
 LPDDR4_DQ4_A <<> DDR DQ4_A H1
 LPDDR4_DQ5_A <<> DDR DQ5_A J2
 LPDDR4_DQ6_A <<> DDR DQ6_A H1
 LPDDR4_DQ7_A <<> DDR DQ7_A H4

LPDDR4_DM0_A <<> DDR DM0_A H5

LPDDR4_DQS0P_A <<> DDR DQS0P_A G1
 LPDDR4_DQS0N_A <<> DDR DQS0N_A G2

LPDDR4_DQ8_A <<> DDR DQ8_A M1
 LPDDR4_DQ9_A <<> DDR DQ9_A N2
 LPDDR4_DQ10_A <<> DDR DQ10_A L7
 LPDDR4_DQ11_A <<> DDR DQ11_A L6
 LPDDR4_DQ12_A <<> DDR DQ12_A K2
 LPDDR4_DQ13_A <<> DDR DQ13_A J6
 LPDDR4_DQ14_A <<> DDR DQ14_A J7
 LPDDR4_DQ15_A <<> DDR DQ15_A L4

LPDDR4_DM1_A <<> DDR DM1_A J4

LPDDR4_DQS1P_A <<> DDR DQS1P_A L2
 LPDDR4_DQS1N_A <<> DDR DQS1N_A L1

LPDDR4_DQ0_B <<> DDR DQ0_B B10
 LPDDR4_DQ1_B <<> DDR DQ1_B A9
 LPDDR4_DQ2_B <<> DDR DQ2_B D12
 LPDDR4_DQ3_B <<> DDR DQ3_B E12
 LPDDR4_DQ4_B <<> DDR DQ4_B A12
 LPDDR4_DQ5_B <<> DDR DQ5_B D15
 LPDDR4_DQ6_B <<> DDR DQ6_B E15
 LPDDR4_DQ7_B <<> DDR DQ7_B E14

LPDDR4_DM0_B <<> DDR DM0_B D14

LPDDR4_DQS0P_B <<> DDR DQS0P_B A11
 LPDDR4_DQS0N_B <<> DDR DQS0N_B B11

LPDDR4_DQ8_B <<> DDR DQ8_B A16
 LPDDR4_DQ9_B <<> DDR DQ9_B B17
 LPDDR4_DQ10_B <<> DDR DQ10_B A17
 LPDDR4_DQ11_B <<> DDR DQ11_B B18
 LPDDR4_DQ12_B <<> DDR DQ12_B B13
 LPDDR4_DQ13_B <<> DDR DQ13_B A13
 LPDDR4_DQ14_B <<> DDR DQ14_B D17
 LPDDR4_DQ15_B <<> DDR DQ15_B B14

LPDDR4_DM1_B <<> DDR DM1_B E17

LPDDR4_DQS1P_B <<> DDR DQS1P_B B15
 LPDDR4_DQS1N_B <<> DDR DQS1N_B B15

X P5
 X M4
 X M5
 X R5
 X M7
 X P4
 X R4

X P7

X P2
 X P1

RK3568
 BGA636_19R00X19R00X1R20

DDR4 LPDDR4 DDR3 LPDDR3

DDR DQ0_A / DDR4 DQ0_L0_A / LPDDR4 DQ0_A / DDR3 DQ0 / LPDDR3 DQ15
 DDR DQ1_A / DDR4 DQ0_L2_A / LPDDR4 DQ1_A / DDR3 DQ1 / LPDDR3 DQ14
 DDR DQ2_A / DDR4 DQ0_L4_A / LPDDR4 DQ2_A / DDR3 DQ2 / LPDDR3 DQ10
 DDR DQ3_A / DDR4 DQ0_L6_A / LPDDR4 DQ3_A / DDR3 DQ3 / LPDDR3 DQ9
 DDR DQ4_A / DDR4 DQ0_L7_A / LPDDR4 DQ4_A / DDR3 DQ4 / LPDDR3 DQ13
 DDR DQ5_A / DDR4 DQ0_L5_A / LPDDR4 DQ5_A / DDR3 DQ5 / LPDDR3 DQ12
 DDR DQ6_A / DDR4 DQ0_L3_A / LPDDR4 DQ6_A / DDR3 DQ6 / LPDDR3 DQ8
 DDR DQ7_A / DDR4 DQ0_L1_A / LPDDR4 DQ7_A / DDR3 DQ7 / LPDDR3 DQ11

DDR DM0_A / DDR4 DML_A / LPDDR4 DM0_A / DDR3 DM0 / LPDDR3 DM1

DDR DQS0P_A / DDR4 DQSL_P_A / LPDDR4 DQS0P_A / DDR3 DQS0P / LPDDR3 DQS1P
 DDR DQS0N_A / DDR4 DQSL_N_A / LPDDR4 DQS0N_A / DDR3 DQS0N / LPDDR3 DQS1N

DDR DQ8_A / DDR4 DQ0_L3_A / LPDDR4 DQ8_A / DDR3 DQ8 / LPDDR3 DQ25
 DDR DQ9_A / DDR4 DQ0_L1_A / LPDDR4 DQ9_A / DDR3 DQ9 / LPDDR3 DQ24
 DDR DQ10_A / DDR4 DQ0_L7_A / LPDDR4 DQ10_A / DDR3 DQ10 / LPDDR3 DQ28
 DDR DQ11_A / DDR4 DQ0_L5_A / LPDDR4 DQ11_A / DDR3 DQ11 / LPDDR3 DQ29
 DDR DQ12_A / DDR4 DQ0_L2_A / LPDDR4 DQ12_A / DDR3 DQ12 / LPDDR3 DQ26
 DDR DQ13_A / DDR4 DQ0_L4_A / LPDDR4 DQ13_A / DDR3 DQ13 / LPDDR3 DQ31
 DDR DQ14_A / DDR4 DQ0_L6_A / LPDDR4 DQ14_A / DDR3 DQ14 / LPDDR3 DQ30
 DDR DQ15_A / DDR4 DQ0_L0_A / LPDDR4 DQ15_A / DDR3 DQ15 / LPDDR3 DQ27

DDR DM1_A / DDR4 DMU_A / LPDDR4 DM1_A / DDR3 DM1 / LPDDR3 DM3

DDR DQS1P_A / DDR4 DQSL_P_A / LPDDR4 DQS1P_A / DDR3 DQS1P / LPDDR3 DQS3P
 DDR DQS1N_A / DDR4 DQSL_N_A / LPDDR4 DQS1N_A / DDR3 DQS1N / LPDDR3 DQS3N

DDR DQ0_B / DDR4 DQ0_L7_B / LPDDR4 DQ0_B / DDR3 DQ16 / LPDDR3 DQ1
 DDR DQ1_B / DDR4 DQ0_L5_B / LPDDR4 DQ1_B / DDR3 DQ17 / LPDDR3 DQ5
 DDR DQ2_B / DDR4 DQ0_L3_B / LPDDR4 DQ2_B / DDR3 DQ18 / LPDDR3 DQ6
 DDR DQ3_B / DDR4 DQ0_L1_B / LPDDR4 DQ3_B / DDR3 DQ19 / LPDDR3 DQ4
 DDR DQ4_B / DDR4 DQ0_L7_B / LPDDR4 DQ4_B / DDR3 DQ20 / LPDDR3 DQ2
 DDR DQ5_B / DDR4 DQ0_L5_B / LPDDR4 DQ5_B / DDR3 DQ21 / LPDDR3 DQ3
 DDR DQ6_B / DDR4 DQ0_L3_B / LPDDR4 DQ6_B / DDR3 DQ22 / LPDDR3 DQ16
 DDR DQ7_B / DDR4 DQ0_L1_B / LPDDR4 DQ7_B / DDR3 DQ23 / LPDDR3 DQ0

DDR DM0_B / DDR4 DMU_B / LPDDR4 DM0_B / DDR3 DM2 / LPDDR3 DM0

DDR DQS0P_B / DDR4 DQSL_P_B / LPDDR4 DQS0P_B / DDR3 DQS2P / LPDDR3 DQS0P
 DDR DQS0N_B / DDR4 DQSL_N_B / LPDDR4 DQS0N_B / DDR3 DQS2N / LPDDR3 DQS0N

DDR DQ8_B / DDR4 DQ0_L0_B / LPDDR4 DQ8_B / DDR3 DQ24 / LPDDR3 DQ18
 DDR DQ9_B / DDR4 DQ0_L2_B / LPDDR4 DQ9_B / DDR3 DQ25 / LPDDR3 DQ19
 DDR DQ10_B / DDR4 DQ0_L4_B / LPDDR4 DQ10_B / DDR3 DQ26 / LPDDR3 DQ22
 DDR DQ11_B / DDR4 DQ0_L6_B / LPDDR4 DQ11_B / DDR3 DQ27 / LPDDR3 DQ23
 DDR DQ12_B / DDR4 DQ0_L7_B / LPDDR4 DQ12_B / DDR3 DQ28 / LPDDR3 DQ16
 DDR DQ13_B / DDR4 DQ0_L5_B / LPDDR4 DQ13_B / DDR3 DQ29 / LPDDR3 DQ17
 DDR DQ14_B / DDR4 DQ0_L3_B / LPDDR4 DQ14_B / DDR3 DQ30 / LPDDR3 DQ30
 DDR DQ15_B / DDR4 DQ0_L1_B / LPDDR4 DQ15_B / DDR3 DQ31 / LPDDR3 DQ21

DDR DM1_B / DDR4 DML_B / LPDDR4 DM1_B / DDR3 DM3 / LPDDR3 DM2

DDR DQS1P_B / DDR4 DQSL_P_B / LPDDR4 DQS1P_B / DDR3 DQS3P / LPDDR3 DQS2P
 DDR DQS1N_B / DDR4 DQSL_N_B / LPDDR4 DQS1N_B / DDR3 DQS3N / LPDDR3 DQS2N

DDR ECC DQ0 / DDR4 ECC DQ0 / -- / DDR3 ECC DQ0
 DDR ECC DQ1 / DDR4 ECC DQ1 / -- / DDR3 ECC DQ1
 DDR ECC DQ2 / DDR4 ECC DQ2 / -- / DDR3 ECC DQ2
 DDR ECC DQ3 / DDR4 ECC DQ3 / -- / DDR3 ECC DQ3
 DDR ECC DQ4 / DDR4 ECC DQ4 / -- / DDR3 ECC DQ4
 DDR ECC DQ5 / DDR4 ECC DQ5 / -- / DDR3 ECC DQ5
 DDR ECC DQ6 / DDR4 ECC DQ6 / -- / DDR3 ECC DQ6
 DDR ECC DQ7 / DDR4 ECC DQ7 / -- / DDR3 ECC DQ7

DDR ECC DM / DDR4 ECC DM / -- / DDR3 ECC DM

DDR ECC DQS / DDR4 ECC DQS_P / -- / DDR3 ECC DQS_P
 DDR ECC DQS / DDR4 ECC DQS_N / -- / DDR3 ECC DQS_N

DDR4 LPDDR4 DDR3 LPDDR3

DDR4 A0 / LPDDR4 CLKP_B / DDR3 A9 / --- / AC0
 DDR4 A1 / --- / DDR3 A2 / --- / AC1
 DDR4 A2 / LPDDR4 A1_A / DDR3 A4 / LPDDR3 A6 / AC2
 DDR4 A3 / LPDDR4 CKEI_A / DDR3 A3 / --- / AC3

DDR4 A4 / LPDDR4 A3_B / DDR3 BA1 / LPDDR3 A3 / AC4
 DDR4 A5 / LPDDR4 A5_B / DDR3 A11 / LPDDR3 A2 / AC5
 DDR4 A6 / LPDDR4 A1_B / DDR3 A13 / LPDDR3 A1 / AC6
 DDR4 A7 / LPDDR4 ODT0_CA_B / DDR3 A8 / --- / AC7

DDR4 A8 / LPDDR4 ODT0_CA_A / DDR3 A6 / LPDDR3 A9 / AC8
 DDR4 A9 / LPDDR4 CLKN_B / DDR3 A5 / --- / AC9
 DDR4 A10 / LPDDR4 CKEO_B / DDR3 A10 / --- / AC10
 DDR4 A11 / LPDDR4 A0_A / DDR3 A7 / LPDDR3 A8 / AC11

DDR4 A12 / LPDDR4 A3_A / DDR3 BA2 / --- / AC12
 DDR4 A13 / LPDDR4 A0_B / DDR3 A14 / LPDDR3 A0 / AC13
 DDR4 A14 WeN / LPDDR4 A4_A / DDR3 A15 / LPDDR3 A5 / AC14
 DDR4 A15 CAsN / LPDDR4 A2_A / DDR3 A0 / --- / AC15

DDR4 A16 RAsN / LPDDR4 A5_A / DDR3 RAsN / LPDDR3 A7 / AC16
 DDR4 ACTn / LPDDR4 CKET_B / DDR3 CAsN / --- / AC17
 DDR4 BA0 / LPDDR4 A2_B / DDR3 A1 / --- / AC18
 DDR4 BA1 / LPDDR4 A4_B / DDR3 A12 / LPDDR3 A4 / AC19

DDR4 BG0 / LPDDR4 ODT1_CA_B / DDR3 WeN / --- / AC20
 DDR4 BG1 / LPDDR4 ODT1_CA_A / DDR3 BA0 / --- / AC21
 DDR4 CKE / LPDDR4 CKEO_A / DDR3 CKE / LPDDR3 CKE / AC22

DDR4 CLKP / LPDDR4 CLKP_A / DDR3 CLKP / LPDDR3 CLKP / AC23
 DDR4 CLKN / LPDDR4 CLKN_A / DDR3 CLKN / LPDDR3 CLKN / AC24

DDR4 CS0n / LPDDR4 CS0n_A / DDR3 ODT1 / LPDDR3 ODT0 / AC25
 DDR4 CS1n / LPDDR4 CS1n_A / DDR3 CS1n / LPDDR3 ODT1 / AC26
 DDR4 ODT0 / LPDDR4 CS1n_B / DDR3 ODT0 / LPDDR3 CS1n / AC27
 DDR4 ODT1 / LPDDR4 CS0n_B / DDR3 CS0n / LPDDR3 CS0n / AC28

DDR4 RESETn / LPDDR4 RESETn / DDR3 RESETn / --- / AC29

Note: Sequences can not be swap

DDR3L =1.35V
 DDR3 =1.5V
 DDR4 =1.2V
 LPDDR3 =1.2V
 LPDDR4 =1.1V
 LPDDR4x =1.1V

DDRPHY_VDDQ_1
 DDRPHY_VDDQ_2
 DDRPHY_VDDQ_3
 DDRPHY_VDDQ_4
 DDRPHY_VDDQ_5
 DDRPHY_VDDQ_6
 DDRPHY_VDDQ_7
 DDRPHY_VDDQ_8

DDR3L =1.35V
 DDR3 =1.5V
 DDR4 =1.2V
 LPDDR3 =1.2V
 LPDDR4 =1.1V
 LPDDR4x =0.6V

DDRPHY_VDDQL_1
 DDRPHY_VDDQL_2
 DDRPHY_VDDQL_3
 DDRPHY_VDDQL_4
 DDRPHY_VDDQL_5
 DDRPHY_VDDQL_6

DDR_AVSS

Note:
 Except DDR3, other DQ sequences
 can not be swap

B6 AC0 >>> LPDDR4_CLKP_B
 F5 AC1 >>> LPDDR4_A1_A
 B1 AC2 >>> LPDDR4_CKE1_A
 F4 AC3 >>> LPDDR4_CKE1_A

D9 AC4 >>> LPDDR4_A3_B
 B7 AC5 >>> LPDDR4_A5_B
 A7 AC6 >>> LPDDR4_A1_B
 A8 AC7 >>> LPDDR4_ODT0_CA_B

C1 AC8 >>> LPDDR4_ODT0_CA_A
 A5 AC9 >>> LPDDR4_CLKN_B
 D6 AC10 >>> LPDDR4_CKE0_B
 C2 AC11 >>> LPDDR4_A0_A

C4 AC12 >>> LPDDR4_A3_A
 B8 AC13 >>> LPDDR4_A0_B
 C5 AC14 >>> LPDDR4_A4_A
 E4 AC15 >>> LPDDR4_A2_A

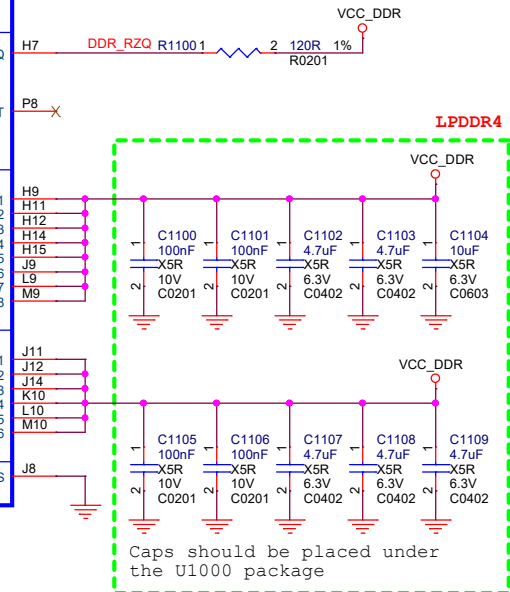
D5 AC16 >>> LPDDR4_A5_A
 E6 AC17 >>> LPDDR4_CKE1_B
 E11 AC18 >>> LPDDR4_A2_B
 E9 AC19 >>> LPDDR4_A4_B

F8 AC20 >>> LPDDR4_CKE0_A
 F7 AC21 >>> LPDDR4_CKE0_A
 B3 AC22 >>> LPDDR4_CKE0_A

B4 AC23 >>> LPDDR4_CLKP_A
 A4 AC24 >>> LPDDR4_CLKN_A

A2 AC25 >>> LPDDR4_CS0n_A
 B2 AC26 >>> LPDDR4_CS1n_A
 E8 AC27 >>> LPDDR4_CS1n_B
 D8 AC28 >>> LPDDR4_CS0n_B

F11 AC29 >>> LPDDR4_RESETn



RK3568_F (DDR PHY)

RK3568_G (OSC/PLL/PMUIO1/2)

U1000G

OSC

XOUT24M

XIN24M

Operating Voltage
=1.8V(PMUPLL_AVDD_1V8)

PMU PLL

PMUPLL_AVDD_0V9

PMUPLL_AVDD_1V8

PMUPLL_AVSS

SYS PLL

SYSPLL_AVDD_0V9

SYSPLL_AVDD_1V8

SYSPLL_AVSS

RK3568
BGA636_19R00X19R00X1R20

PMUIO1 Domain

Operating Voltage=3.3V Only

PMUIO2 Domain

Operating Voltage=1.8V/3.3V

PMUIO1/2/OSC Domain Logic Power

Operating Voltage=0.9V

PMU_VDD_LOGIC_0V9

NPOR_u

PMUIO1

PMUIO2

AH27

AG27

AG26

AG28

AA22

Y22

AF25

AE24

Y20

AD23

AF24

AB21

AG24

AB20

AC22

AA20

AH26

AD22

AF23

AG23

AE23

AD21

AC21

AD20

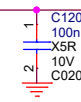
AH25

AC20

AH24

W19

V19



TSADC_SHUT_M0

REFCLK_OUT_CAM

PMIC_SLEEP_H

PMIC_INT_L

SDMMC0_DET_L

WL_EN_GPIO0_A5

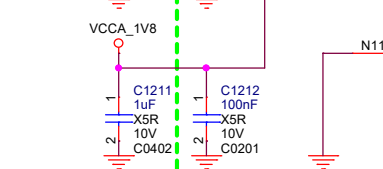
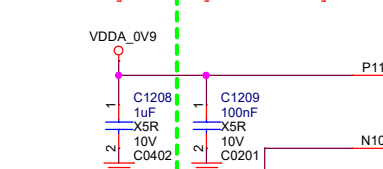
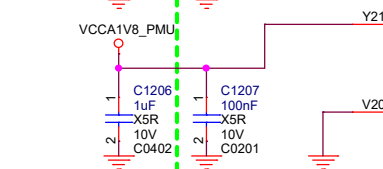
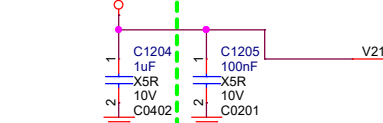
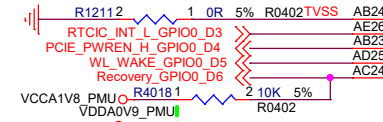
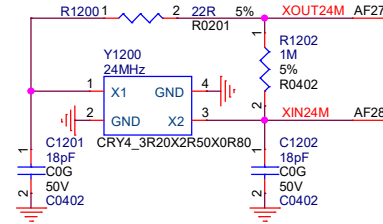
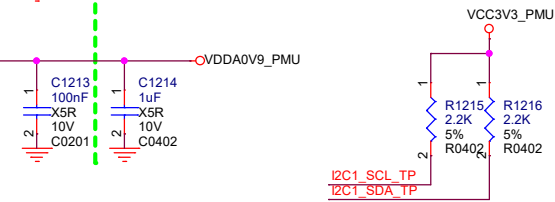
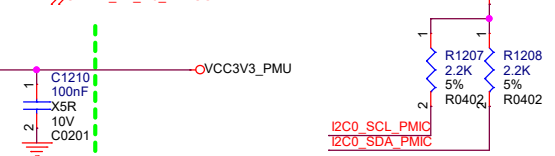
XGMAC1_INT_GPIO0_A6

VCC3V3_PMU

CLK32K_OUT0
X2C0_SCL_PMIC
X2C0_SDA_PMIC
X2C1_SCL_TP
X2C1_SDA_TP
TP_INT_L_GPIO0_B5
TP_RST_L_GPIO0_B6
M2_WAKE_GPIO0_B7

WORKING_LEDEN_H_GPIO0_C0
WAKEUP_MINIPIC_GPIO0_C1
EDP_HPDI_GPIO0_C2
LCD0_BL_PWM4
LCD1_BL_PWM5
minIPIC_PWREN_H_GPIO0_C5
PWM7_IR
LCD0_PWREN_H_GPIO0_C7

VCC3V3_PMU



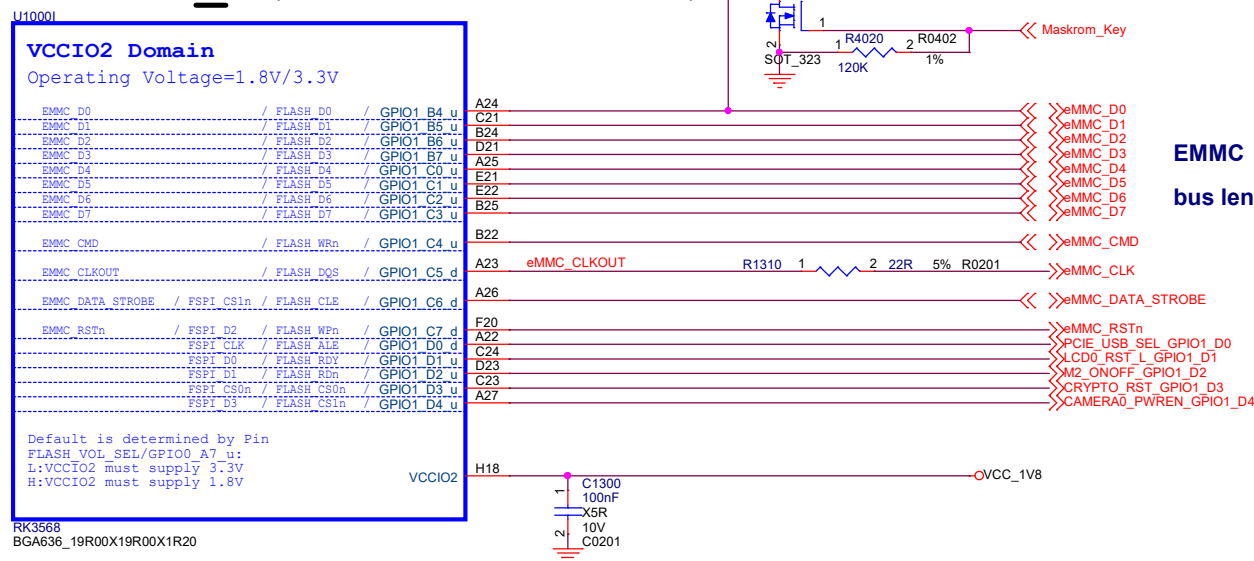
Caps should be placed close to the U1000 package

Caps should be placed under the U1000 package



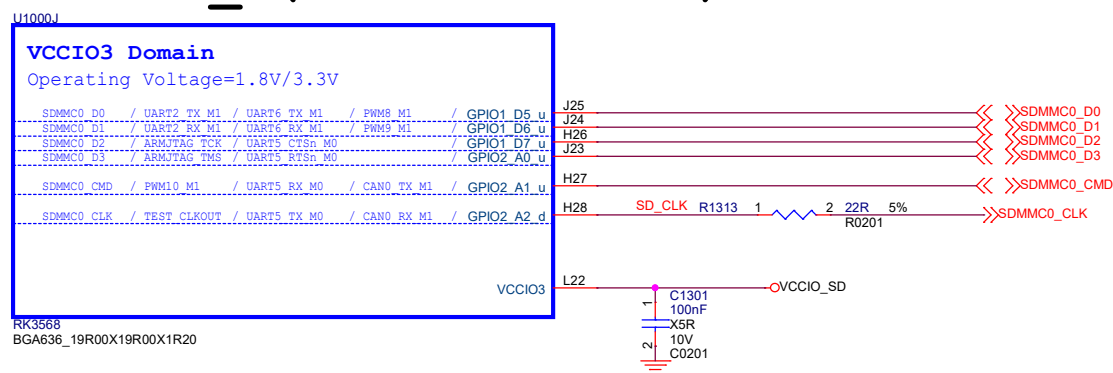
Design Name		Mixtile-Core-3568	
Size	B	Page Name	06-RK3568 OSC PLL PMUIO
Date:	Friday, May 06, 2022	Rev	V1.2.0
Sheet		6 of 17	

RK3568_I (VCCIO2 Domain)

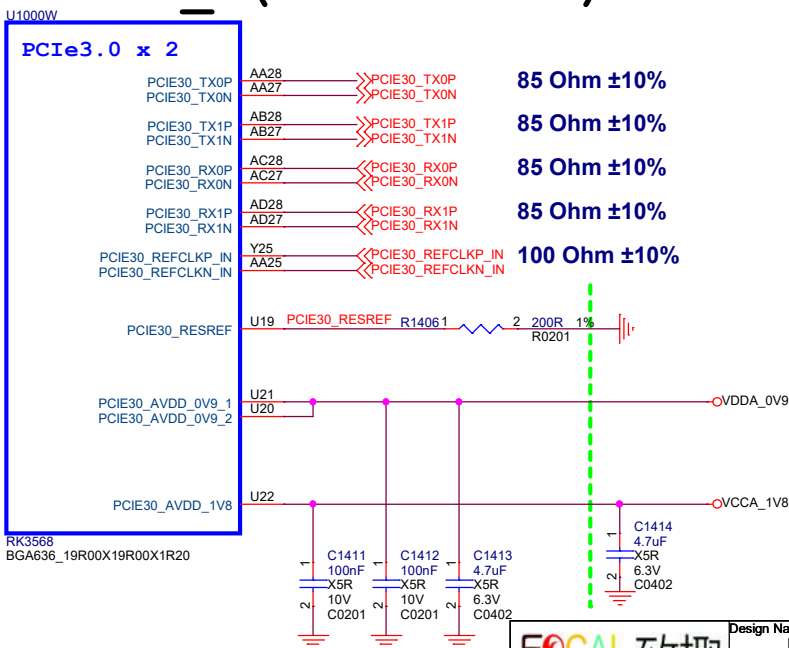
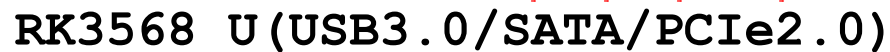


EMMC trace single-ended 50 Ohm $\pm 10\%$
bus length tolerance limit in 10mil

RK3568_J (VCCIO3 Domain)



SDC trace single-ended 50 Ohm $\pm 10\%$
bus length tolerance limit in 10mil



VCCIO4 Domain									
Operating Voltage=1.8V/3.3V									
SDMMC1 D0	/	GMACO RYD2	/	UART6 RX M0	/	GPIO2 A3			
SDMMC1 D1	/	GMACO RXD3	/	UART6 TX M0	/	GPIO2 A4 u			
SDMMC1 D2	/	GMACO RXCLK	/	UART7 RX M0	/	GPIO2 A5 u			
SDMMC1 D3	/	GMACO TXD2	/	UART7 TX M0	/	GPIO2 A6 u			
SDMMC1 CMD	/	GMACO TXD3	/	UART9 RX M0	/	GPIO2 A7 u			
SDMMC1 CLK	/	GMACO TXCLK	/	UART9 TX M0	/	GPIO2 B0 d			
SDMMC1 PWREN	/	I2C4 SDA M1	/	UART8 RTSn M0	/	CAN2 RX M1	/	GPIO2 B1 d	
SDMMC1 DET	/	I2C4 SCL M1	/	UART6 CTSn M0	/	CAN2 TX M1	/	GPIO2 B2 u	
		GMACO TXD0	/	UART1 RX M0	/	GPIO2 B3 u			
		GMACO TXD1	/	UART1 TX M0	/	GPIO2 B4 u			
		GMACO TXEN	/	UART1 RTSn M0	/	SPI1 CLK M0	/	GPIO2 B5 u	
		GMACO RXD0	/	UART1 CTSn M0	/	SPI1 MISO M0	/	GPIO2 B6 u	
I2S2 SCLK RX M0	/	GMACO RXD1	/	UART6 RTSn M0	/	SPI1 MOSI M0	/	GPIO2 B7 d	
I2S2 LRCK RX M0	/	GMACO RXD0 CRS	/	UART6 CTSn M0	/	SPI1 CS0 M0	/	GPIO2 C0 d	
I2S2 MCLK M0	/	ETH0 REFCLK0 ZSM	/	UART7 RTSn M0	/	SPI2 CLK M0	/	GPIO2 C1 d	
I2S2 SCLK TX M0	/	GMACO MCLKINOUT	/	UART7 CTSn M0	/	SPI2 MISO M0	/	GPIO2 C2 d	
I2S2 LRCK TX M0	/	GMACO MDC	/	UART9 RTSn M0	/	SPI2 MOSI M0	/	GPIO2 C3 d	
I2S2 SDO M0	/	GMACO MDIO	/	UART9 CTSn M0	/	SPI2 CS0 M0	/	GPIO2 C4 d	
I2S2 SDI M0	/	GMACO RXER	/	UART6 TX M0	/	SPI2 CS1 M0	/	GPIO2 C5 d	
CLK32K OUT1	/		/	UART8 RX M0	/	SPI1 CS1 M0	/	GPIO2 C6 d	

VCCIO4

RK3568
BGA636 19R00X19R00X1R20

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U1000N
VCCIO7 Domain
Operating Voltage=1.8V/3.3V

PWM14 M1 / SPI3 CLK M1 / CAN1 RX M1 / PCIE30X2 CLKREQ# M2 / I2S3 MCLK M1 / GPIO4 C2 d
PWM15 TR M1 / SPI3 MOSI M1 / CAN1 TX M1 / PCIE30X2 WAKE# M2 / I2S3 SCLK M1 / GPIO4 C3 d
EDP HPDIN M0 / SPDIF TX M2 / SATA2 ACT LED / PCIE30X2 PERSTn M2 / I2S3 LRCK M1 / GPIO4 C4 d
PWM12 M1 / SPI3 MISO M1 / SATA1 ACT LED / UART9 TX M1 / I2S3 SDO M1 / GPIO4 C5 d
PWM13 M1 / SPI3 CS0 M1 / SATA0 ACT LED / UART9 TX M1 / I2S3 SDT M1 / GPIO4 C6 d

HDMITX SCL / I2C5 SCL M1 / GPIO4 C7 u
HDMITX SDA / I2C5 SDA M1 / GPIO4 D0 u
HDMITX CEC M0 / SPI3 CS1 M1 / GPIO4 D1 u

GPIO4 D2 d

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RK3568
BGA636 19R00X19R00X1R20

Diagram illustrating the pin connections for the STM32F405VGT6 microcontroller to the BT module. The connections are as follows:

- E27 (R4015) to GMAC0_RXD2
- E28 (R4014) to GMAC0_RXD3
- B28 (R4014) to GMAC0_RXD3
- C27 (R4015) to GMAC0_RXCLK
- C27 (R4015) to GMAC0_TXD2
- C28 (R4014) to GMAC0_TXD3
- D27 (R4017) to GMAC0_TXCLK
- D26 (R4017) to GMAC0_TXCLK
- E25 (R4017) to UART8_RTSn_M0 and UART8_CTSn_M0 (For BT)
- F28 (R4013) to GMAC0_TXD0
- G27 (R4012) to GMAC0_TXD1
- G28 (R4016) to GMAC0_TXEN
- F27 (R4016) to GMAC0_RXD0
- H25 (R4016) to GMAC0_RXD1
- F24 (R4016) to GMAC0_RXDV_CRS
- G23 (R1515) to ETH0_REFCLK_25M
- F25 (R4016) to GMAC0_MCLKINOUT
- H24 (R4016) to GMAC0_MDC
- H23 (R4016) to GMAC0_MDIO
- F26 (R4016) to UART8_TX_M0
- E26 (R4016) to UART8_RX_M0 (For BT)

Power supply connections:

- J21 (VCC_1V8) to C1510 (100nF), X5R (10V), and C0201.

U10000

SARADC
Recovery

SARADC_VIN0
SARADC_VIN1
SARADC_VIN2
SARADC_VIN3
SARADC_VIN4
SARADC_VIN5
SARADC_VIN6
SARADC_VIN7

SARADC_AVDD_1V8
OTP_VCC18

OTF

B27 SARADC_VIN0_KEY/RECOVERY C1501 1 2 1nF X5R 50V C0402
C26 SARADC_VIN1_EVB_HW_ID C1501 1 2 1nF X5R 50V C0402
D24 SARADC_VIN2_LCD_ID C1502 1 2 1nF X5R 50V C0402
E23 SARADC_VIN3 C1503 1 2 1nF X5R 50V C0402
G21 SARADC_VIN4 C1504 1 2 1nF X5R 50V C0402
F22 SARADC_VIN5 C1505 1 2 1nF X5R 50V C0402
G20 SARADC_VIN6 C1506 1 2 1nF X5R 50V C0402
F21 SARADC_VIN7 C1507 1 2 1nF X5R 50V C0402

H22 SARADC_AVDD_1V8
H20 OTP_VCC18

C1508 100nF X5R 10V C0201
C1509 100nF X5R 10V C0201

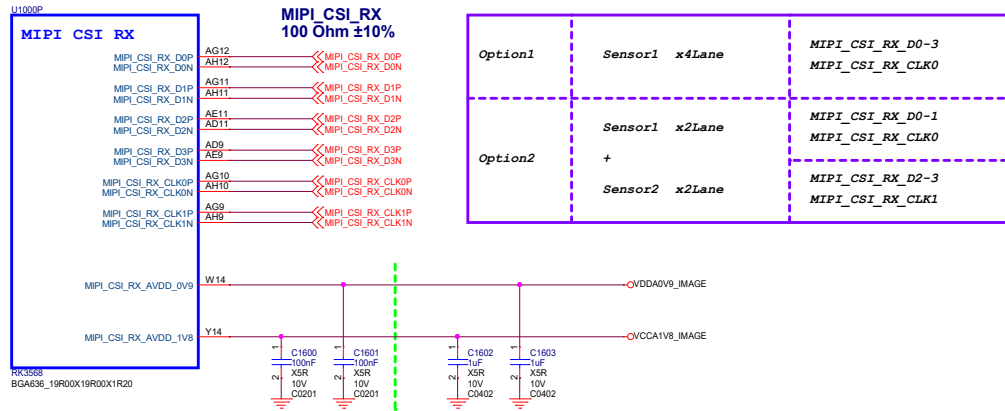
VCCA_1V8
VCC_1V8

BGA636_19R00X19R00X1R20

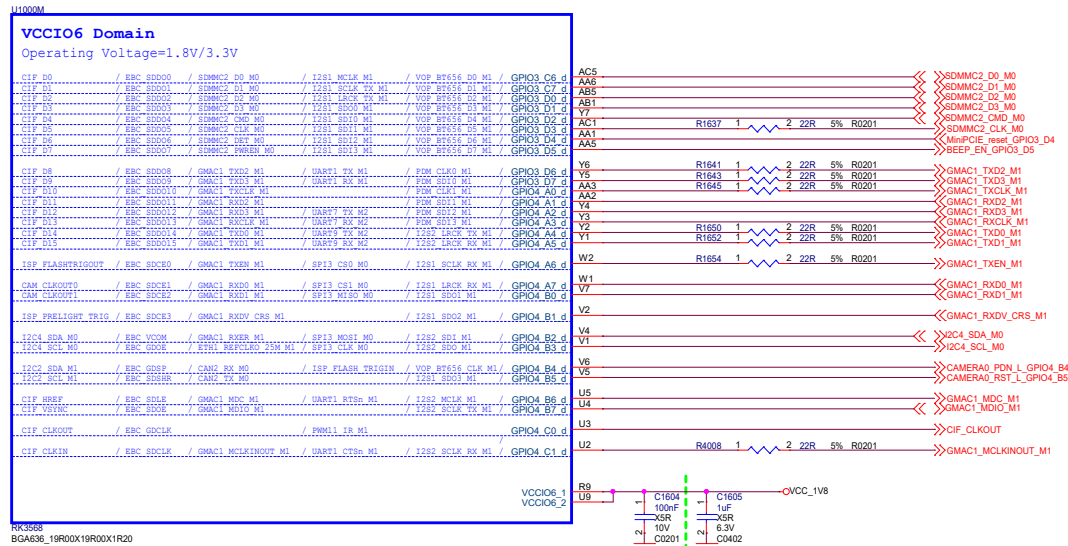
RK3568
BGA636 19R00X19R00X1R20

SARADC_VINO_KEY/RECOVERY	>> SARADC_VIN0_KEY/RECOVERY	2	1000000	2	1000000
SARADC_VIN1_EVB_HW_ID	>> SARADC_VIN1_EVB_HW_ID				
SARADC_VIN2_LCD_ID	>> SARADC_VIN2_LCD_ID				
SARADC_VIN3	>> SARADC_VIN3				
SARADC_VIN4	>> SARADC_VIN4				
SARADC_VIN5	>> SARADC_VIN5				
SARADC_VIN6	>> SARADC_VIN6				
SARADC_VIN7	>> SARADC_VIN7				

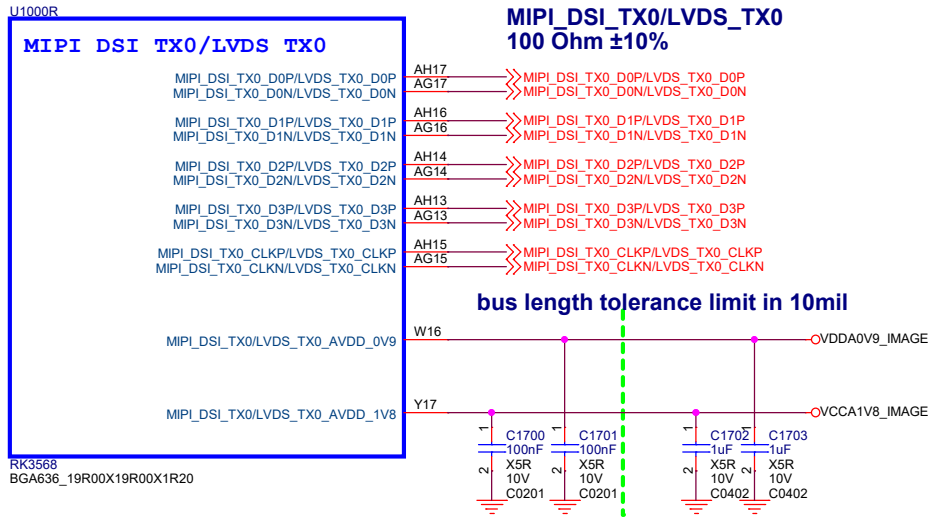
RK3568_P (MIPI_CSI_RX)



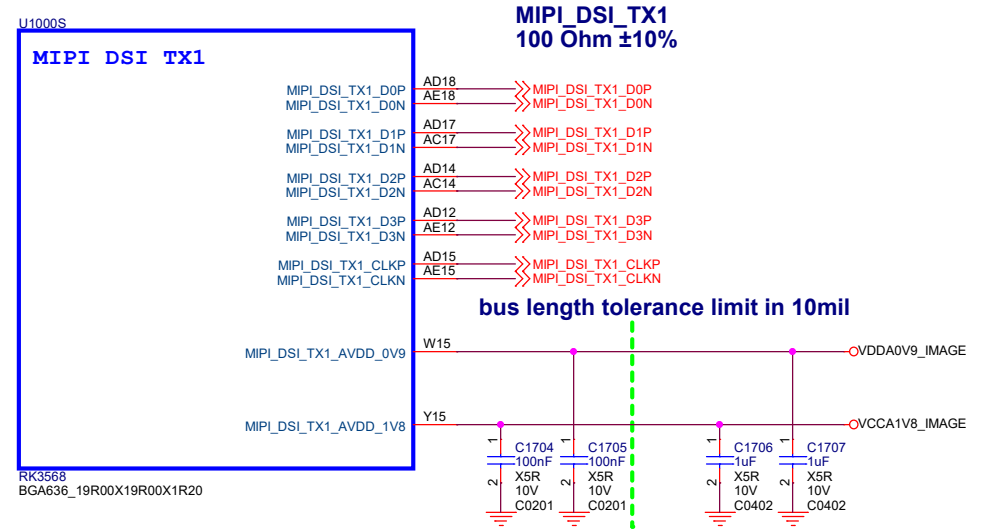
RK3568_M (VCCIO6 Domain)



RK3568_R(MIPI_DSI_TX0/LVDS_TX0)

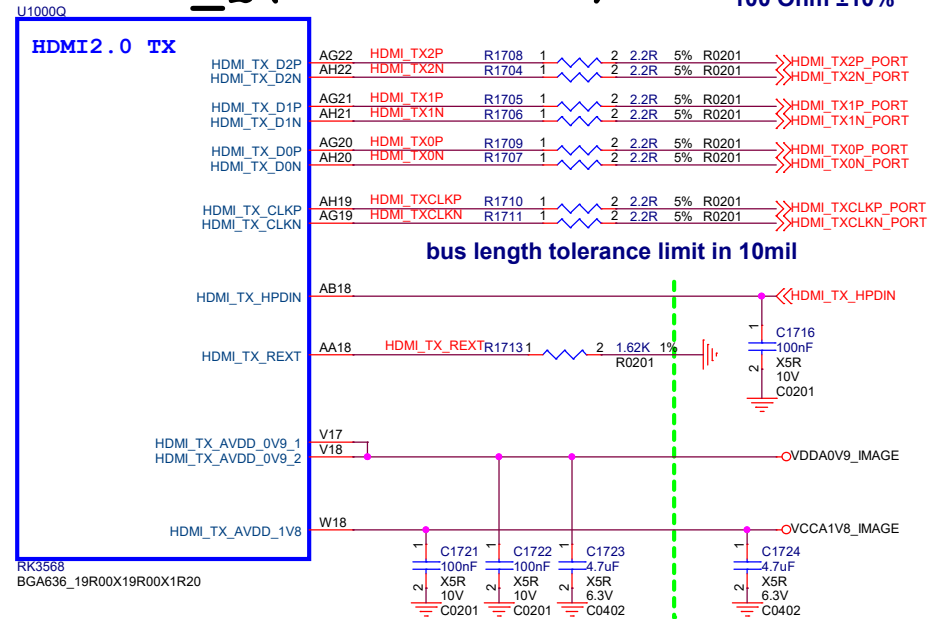


RK3568_S(MIPI_DSI_TX1)



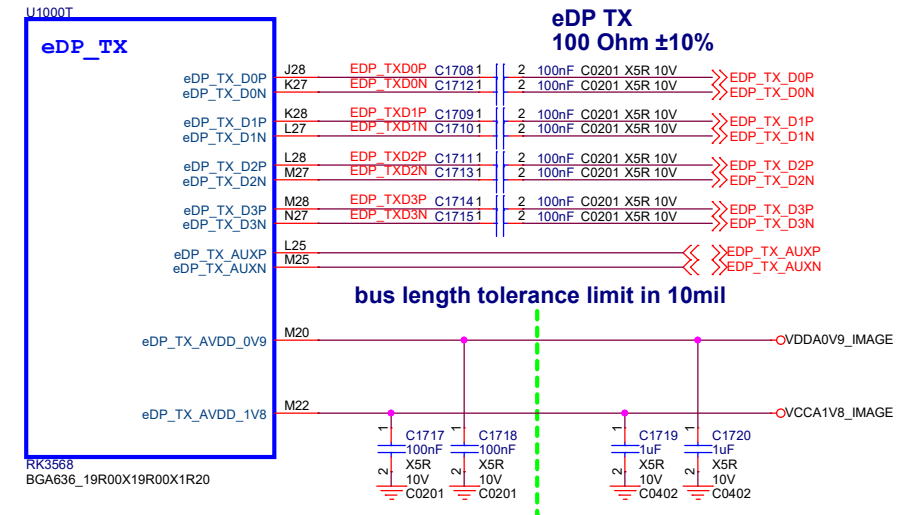
RK3568_Q(HDMI2.0 TX)

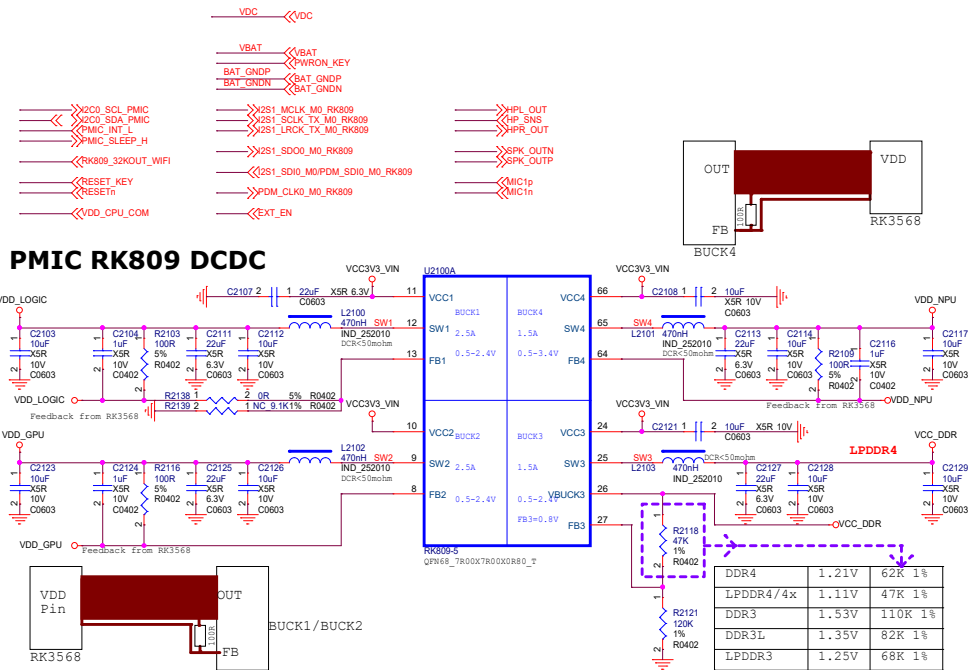
HDMI TMDs trace
100 Ohm ±10%



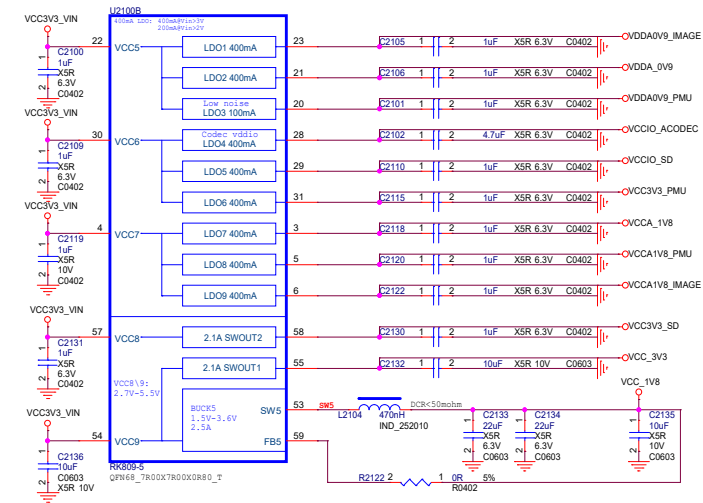
RK3568_T(eDP TX)

eDP TX
100 Ohm ±10%

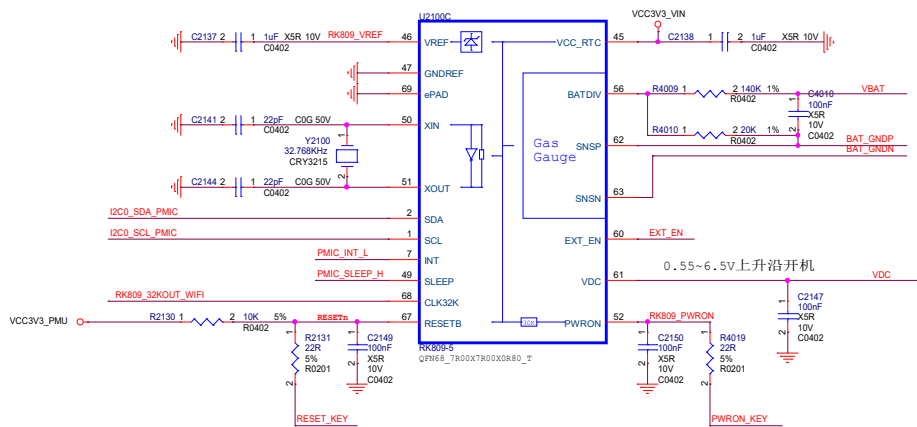




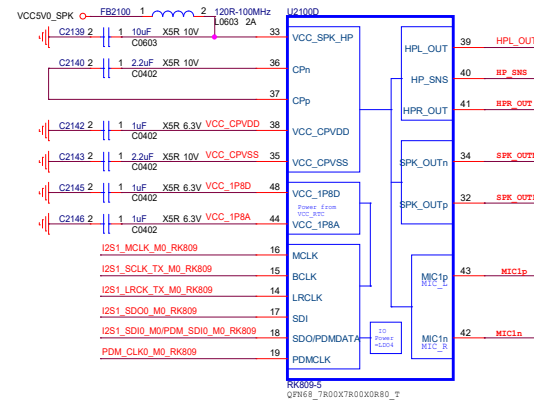
PMIC RK809 LDO



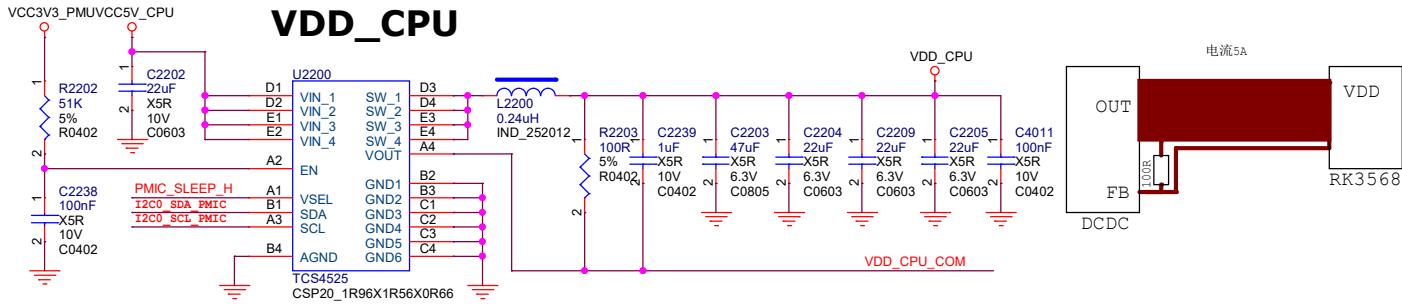
PMIC RK809 Management



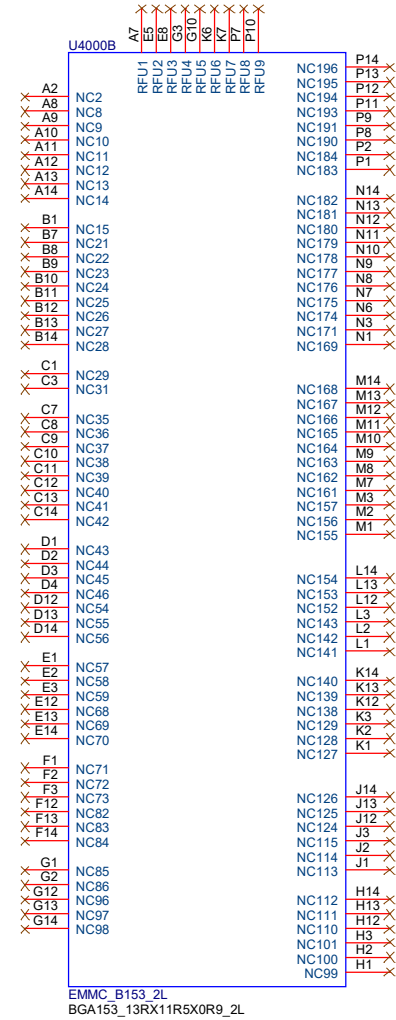
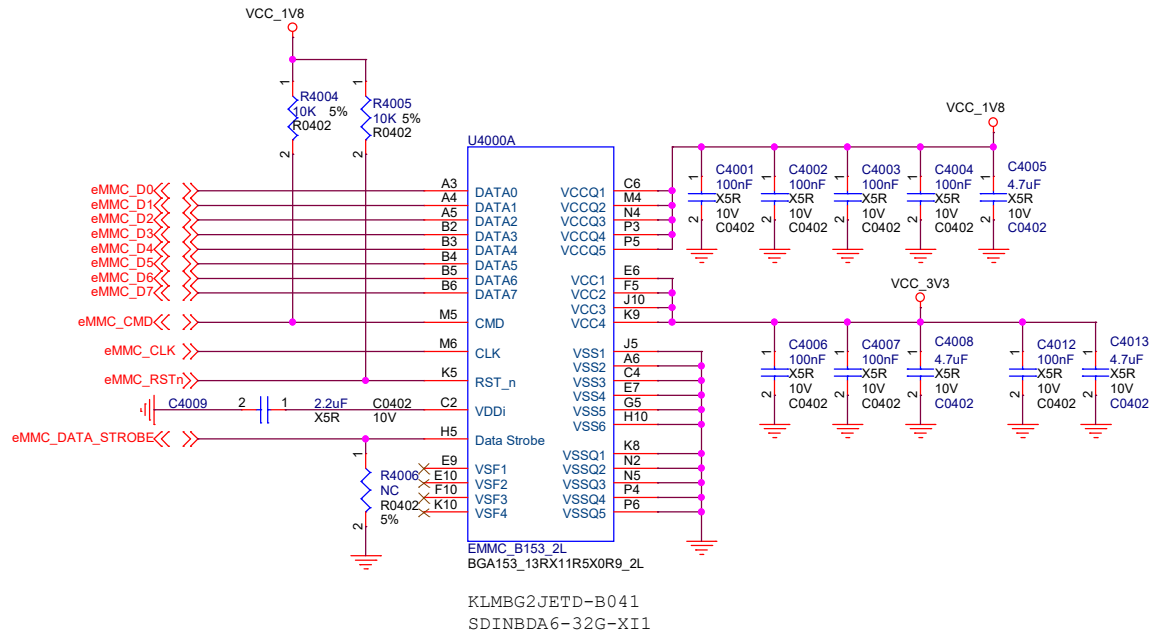
PMIC RK809 CODEC



>>PMIC_SLEEP_H
>>VDD_CPU_COM
<<I2C0_SCL_PMIC
<<I2C0_SDA_PMIC



Design Name		
Mixtile-Core-3568		
Size	Page Name	Rev
B	14-Power DCDC	V1.2.0
Date:	Friday, May 06, 2022	Sheet 14 of 17



Design Name			
Mixtile-Core-3568			
Size	Page Name	Rev	
B	16-Flash eMMC	V1.2.0	
Date:	Friday, May 06, 2022	Sheet	16 of 17

